Features

- Supply Voltage up to 40V
- R_{DSon} Typically 0.8Ω at 25°C, Maximum 1.8Ω at 200°C
- Up to 1.0A Output Current
- Three Half-bridge Outputs Formed by Three High-side and Three Low-side Drivers
- Capable of Switching Loads such as DC Motors, Bulbs, Resistors, Capacitors, and Inductors
- PWM Capability up to 25 kHz for Each High-side Output Controlled by External PWM Signal
- No Shoot-through Current
- Outputs Short-circuit Protected
- Selective Overtemperature Protection for Each Switch and Overtemperature Prewarning
- Undervoltage Protection
- Various Diagnostic Functions such as Shorted Output, Open Load, Overtemperature and Power-supply Fail Detection
- Serial Data Interface, Daisy Chain Capable, up to 2 MHz Clock Frequency
- QFN18 Package

High Temperature Triple Half-bridge Driver with SPI and PWM

ATA6832

1. Description

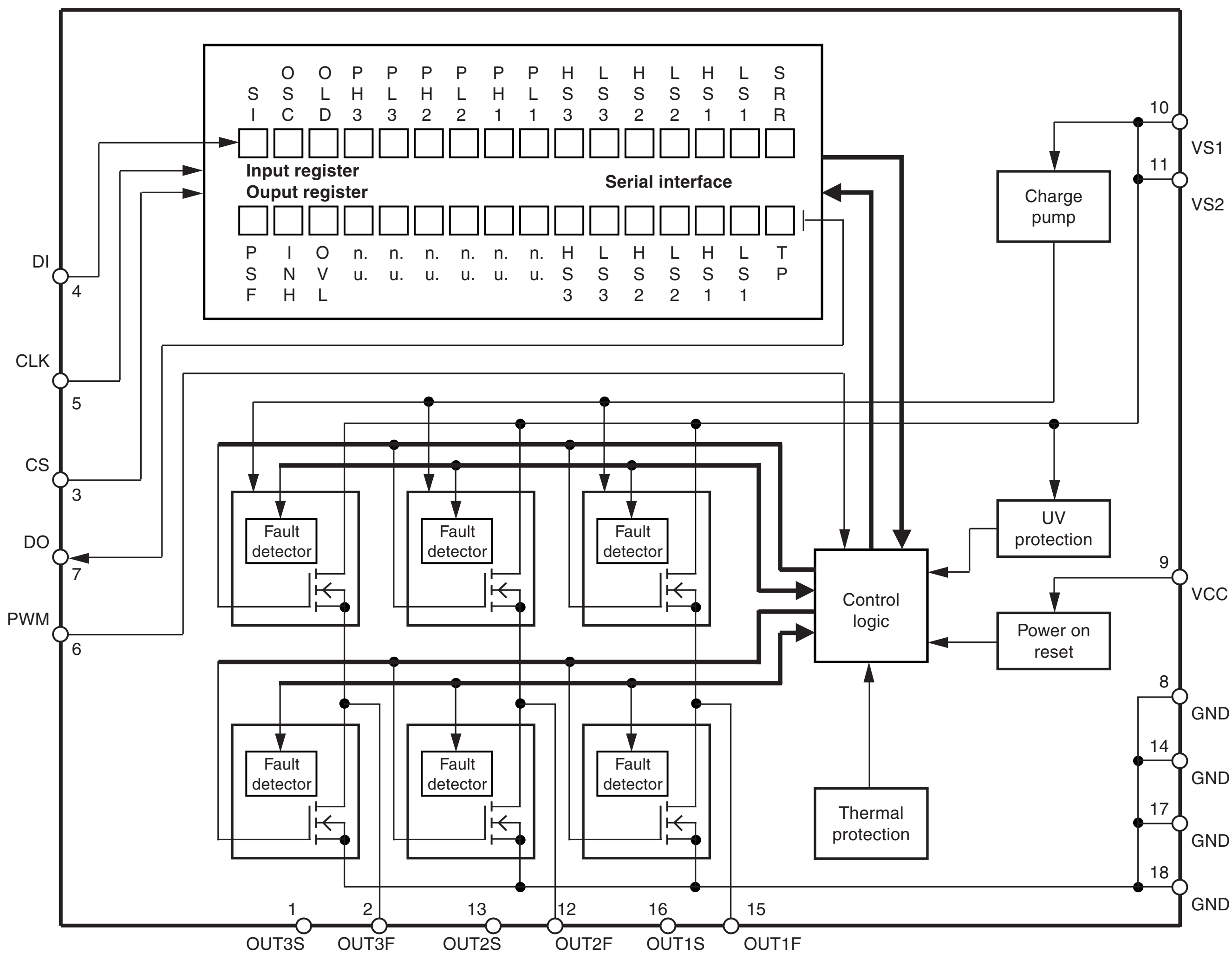
The ATA6832 is a fully protected driver IC specially designed for high temperature applications. In mechatronic solutions, for example turbo charger or exhaust gas recirculation systems, many flaps have to be controlled by DC motor driver ICs which are located very close to the hot engine or actuator where ambient temperatures up to 150°C are usual. Due to the advantages of SOI technology junction temperatures up to 200°C are allowed. This enables new cost effective board design possibilities to achieve complex mechatronic solutions.

The ATA6832 is a triple half-bridge driver to control up to 3 different loads by a microcontroller in automotive and industrial applications. Each of the 3 high-side and 3 low-side drivers is capable of driving currents up to 1.0A. Due to the enhanced PWM signal (up to 25 kHz) it is possible to generate a smooth control of, for example, a DC motor without any noise. The drivers are internally connected to form 3 half-bridges and can be controlled separately from a standard serial data interface, enabling all kinds of loads, such as bulbs, resistors, capacitors and inductors, to be combined. The IC design especially supports the application of H-bridges to drive DC motors.

Protection is guaranteed with respect to short-circuit conditions, overtemperature and undervoltage. Various diagnostic functions and a very low quiescent current in standby mode enable a wide range of applications. Automotive qualification (protection against conducted interferences, EMC protection and 1.5-kV ESD protection) gives added value and enhanced quality for exacting requirements of automotive applications.

4951E–AUTO–02/10

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN24

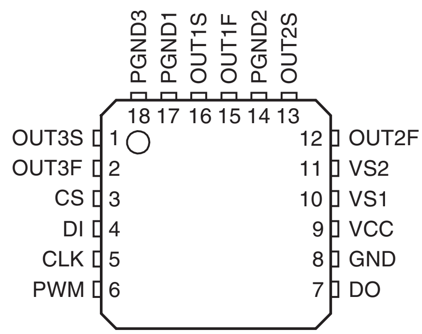


Table 2-1.

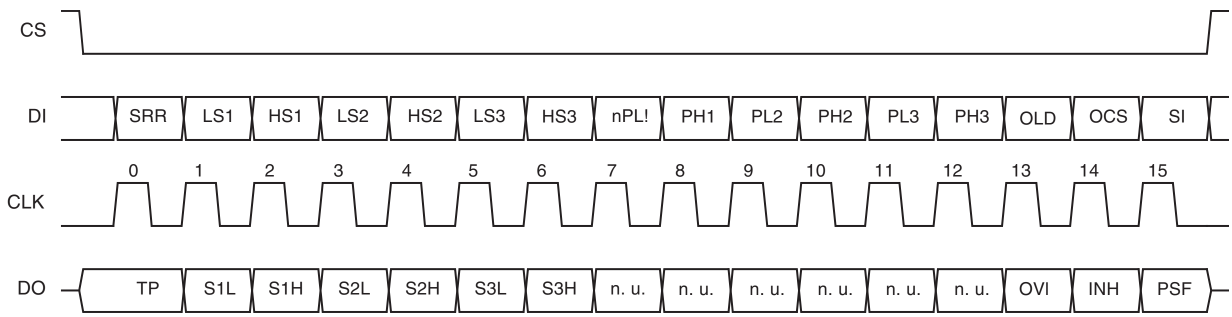
Pin	Symbol	Function
1	OUT3S	Used only for final testing, to be connected to OUT3F
2	OUT3F	Half-bridge output 3; formed by internally connecting power MOS high-side switch 3 and low-side switch 3 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load
3	CS	Chip select input; 5V CMOS logic level input with internal pull-up; low = serial communication is enabled, high = disabled
4	DI	Serial data input; 5V CMOS logic level input with internal pull-down; receives serial data from the control device; DI expects a 16-bit control word with LSB transferred first
5	CLK	Serial clock input; 5V CMOS logic level input with internal pull-down; controls serial data input interface and internal shift register (f_{max} = 2 MHz)
6	PWM	PWM input; 5V CMOS logic level input with internal pull-down
7	DO	Serial data output; 5V CMOS logic-level tri-state output for output (status) register data; sends 16-bit status information to the microcontroller (LSB transferred first); output will remain tri-stated unless device is selected by CS = low; this allows several ICs to operate on only one data-output line
8	GND	Ground
9	VCC	Logic supply voltage (5V)
10	VS1	Power supply for output stages OUT1 and OUT2; internal supply
11	VS2	Power supply for output stages OUT2 and OUT3; internal supply
12	OUT2F	Half-bridge output 2; formed by internally connected power MOS high-side switch 2 and low-side switch 2 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load
13	OUT2S	Used only for final testing, to be connected to OUT2F
14	PGND2	Power ground OUT2
15	OUT1F	Half-bridge output 1; formed by internally connected power MOS high-side switch 1 and low-side switch 1 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load
16	OUT1S	Used only for final testing, to be connected to OUT1F
17	PGND1	Power ground OUT1
18	PGND3	Power ground OUT3

3. Functional Description

3.1 Serial Interface

to CLK and is accepted on the falling edge of the CLK signal. The LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, pin DO is in tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Data Transfer



Input Data Protocol

0	SRR	Status register reset (high = reset; the bits PSF and OVL in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	PL1	Output LS1 additionally controlled by PWM Input
8	PH1	Output HS1 additionally controlled by PWM Input
9	PL2	See PL1
10	PH2	See PH1
11	PL3	See PL1
12	PH3	See PH1
13	OLD	Open load detection (low = on)
14	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by the standby function because the digital part is still powered)

Output Data Protocol

	Output (Status) Register	Function
		Temperature prewarning: high = warning
1	Status LS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR
2	Status HS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	OVL	Over-load detected: set high, when at least one output is switched off by a short-circuit condition or an overtemperature event. Bits 1 to 6 can be used to detect the affected switch
14	INH	Inhibit: this bit is controlled by software (bit SI in input register) High = standby, low = normal operation
15	PSF	Power-supply fail: undervoltage at pin VS detected

After power-on reset, the input register has the following status:

		Bit 13 OLD	Bit 12 PH3	Bit 11 PL3	Bit 10 PH2	Bit 9 PL2	Bit 8 PH1	Bit 7 PL1	Bit 6 HS3	Bit 5 LS3	Bit 4 HS2	Bit 3 LS2	Bit 2 HS1	Bit 1 LS1	Bit 0 SRR

The following patterns are used to enable internal test modes of the IC. Do not use these patterns during normal operation.

Bit 15	Bit 14	Bit 13 (OCS)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)

3.2 Power-supply Fail

$_{dUV}$. The outputs are enabled immediately when the supply voltage returns to the normal operational value. The PSF bit stays high until it is reset by the SRR bit in the input register.

Open-load Detection

$_{OUT1-3}$). If the current through the external load does not reach the open-load detection current, the corresponding bit of the output in the output register is set to high.

Switching on an output stage with the OLD bit set to low disables the open-load function for this output.

3.4 Overtemperature Protection

$_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold, $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word. The status of TP is available at pin DO with the falling edge of CS. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the status of input and output registers.

If the junction temperature of an output stage exceeds the thermal shutdown threshold, $T_{jswitch\ off}$, the affected output is disabled and the corresponding bit in the output register is set to low. Additionally, the overload detection bit (OVL) in the output register is set. The output can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{jswitch\ on}$, and the SRR bit in the input register is set to high. The hysteresis of thermal prewarning and shutdown threshold avoids oscillations.

3.5 Short-circuit Protection

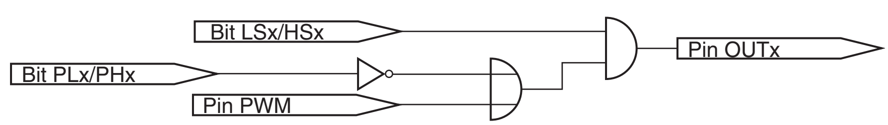
$_{dSd}$). The over-load detection bit (OVL) is set and the corresponding status bit in the output register is set to low. For OCS = low, the overcurrent shutdown is inactive and the OVL bit is not set by an overcurrent. By writing a high to the SRR bit in the input register the OVL bit is reset and the disabled outputs are enabled.

3.6 Inhibit

put stages can be reactivated by setting bit SI to “1”.

3.7 PWM Mode

Figure 3-2.



4. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply voltage	10, 11	V_{VS}	–0.3 to +40	V
Supply voltage $t < 0.5s$; $I_S > –2A$	10, 11	V_{VS}	–1	V
Logic supply voltage	9	V_{VCC}	–0.3 to +7	V
Logic input voltage	3, 4, 5, 6	V_{CS}, V_{DI}, V_{CLK}, V_{PWM}	–0.3 to V_{VCC} + 0.3	V
Logic output voltage	7	V_{DO}	–0.3 to V_{VCC} + 0.3	V
Input current	3, 4, 5, 6	I_{CS}, I_{DI}, I_{CLK}, I_{PWM}	–10 to +10	mA
Output current	7	I_{DO}	–10 to +10	mA
Output current	2, 12, 15	I_{Out1}, I_{Out2}, I_{Out3}	Internally limited, see output specification	
Output voltage	2, 12, 15	I_{Out1}, I_{Out2}, I_{Out3}	–0.3 to +40	V
Reverse conducting current (t_{pulse} = 150 µs)	2, 12, 15	I_{Out1}, I_{Out2}, I_{Out3}	17	A
Junction temperature range		T_j	–40 to +200	°C
Storage temperature range		T_{STG}	–55 to +200	°C
Ambient temperature range		T_a	–40 to +150	°C

5. Thermal Resistance

Parameters	Test Conditions	Symbol	Value	Unit
Thermal resistance from junction to case		R_{thJC}	5	k/W
Thermal resistance from junction to ambient	Depends on the PC board	R_{thJA}	40	K/W

6. Operating Range

Parameters	Symbol	Value	Unit
		$_{UV}$[1] to 40	V
Logic supply voltage	V_{VCC}	4.75 to 5.25	V
Logic input voltage	V_{CS}, V_{DI}, V_{CLK}, V_{PWM}	–0.3 to V_{VCC}	V
Serial interface clock frequency	f_{CLK}	2	MHz
PWM input frequency	f_{PWM}	max. 25	kHz
Junction temperature range	T_j	–40 to +150	°C

Note: 1. Threshold for undervoltage description

7. Noise and Surge Immunity

Parameters	Test Conditions	Value

8. Electrical Characteristics

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Current Consumption**								
	Quiescent current VS	V_{VS} < 20V, SI = low	10, 11	I_{VS}		1	60	µA	A
1.2	Quiescent current VCC	4.75V < V_{VCC} < 5.25V, SI = low	9	I_{VCC}		60	160	µA	A
1.3	Supply current VS	V_{VS} < 20V normal operating, all outputs off, input register bit 13 (OLD) = high	10, 11	I_{VS}		4	6	mA	A
1.4	Supply current VCC	4.75V < V_{VCC} < 5.25V, normal operating	9	I_{VCC}		350	650	µA	A
1.5	Discharge current VS	V_{VS} = 32.5V, INH = low	10, 11	I_{VS}	0.5		5.5	mA	A
1.6	Discharge current VS	V_{VS} = 40V, INH = low	10, 11	I_{VS}	2.0		14	mA	A
2	**Undervoltage Detection, Power-on Reset**								
2.1	Power-on reset threshold		9	V_{VCC}	3.1	3.9	4.5	V	A
2.2	Power-on reset delay time	After switching on V_{CC}		t_{dPor}	30	95	190	µs	A
2.3	Undervoltage-detection threshold	V_{CC} = 5V	10, 11	V_{Uv}	5.5		7.1	V	A
2.4	Undervoltage-detection hysteresis	V_{CC} = 5V	10, 11	ΔV_{Uv}		0.6		V	A
2.5	Undervoltage-detection delay time			t_{dUV}	10		40	µs	A
3.1	Thermal prewarning set			$T_{jPW\ set}$	170	195	220	°C	B
3.2	Thermal prewarning reset			$T_{jPW\ reset}$	155	180	205	°C	B
3.3	Thermal prewarning hysteresis			ΔT_{jPW}		15		K	B
3.4	Thermal shutdown off			$T_{j\ switch\ off}$	200	225	250	°C	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1 ms.
2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

8. Electrical Characteristics (Continued)

≤ ≤ ≤

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.5	Thermal shutdown on			$T_{j\ switch\ on}$	185	210	235	°C	B
3.6	Thermal shutdown hysteresis			$\Delta T_{j\ switch\ off}$		15		K	B
3.7	Ratio thermal shutdown off/thermal prewarning set			$T_{j\ switch\ off}/T_{jPW\ set}$	1.05	1.2			B
3.8	Ratio thermal shutdown on/thermal prewarning reset			$T_{j\ switch\ on}/T_{jPW\ reset}$	1.05	1.2			B
4.1	On resistance	$I_{Out\ 1\text{-}3} = -0.9$ A	2, 12, 15	$R_{DSon1\text{-}3H}$			1.8	Ω	A
4.2		$I_{Out\ 1\text{-}3} = -0.9$ A	2, 12, 15	$R_{DSon1\text{-}3L}$			1.8	Ω	A
4.3	High-side output leakage current	$V_{Out\ 1\text{-}3\ H} = 0V$, output stages off	2, 12, 15	$I_{Out1\text{-}3H}$	–60			µA	A
4.4	Low-side output leakage current	$V_{Out\ 1\text{-}3\ L} = V_{VS}$, output stages off	2, 12, 15	$I_{Out1\text{-}3L}$			300	µA	A
4.5	High-side switch reverse diode forward voltage	$I_{Out} = 1.5A$	2, 12, 15	$V_{Out1\text{-}3} - V_{VS}$			2	V	A
4.6	Low-side switch reverse diode forward voltage	$I_{Out\ 1\text{-}3\ L} = -1.5A$	2, 12, 15	$V_{Out1\text{-}3L}$	2			V	A
4.7	High-side overcurrent limitation and shutdown threshold	$7.5V < V_{VS} < 20V$	2, 12, 15	$I_{Out1\text{-}3}$	1.0	1.3	1.7	A	A
4.8	Low-side overcurrent limitation and shutdown threshold	$7.5V < V_{VS} < 20V$	2, 12, 15	$I_{Out1\text{-}3}$	–1.7	–1.3	–1.0	A	A
4.9	High-side overcurrent limitation and shutdown threshold	$20V < V_{VS} < 40V$	2, 12, 15	$I_{Out1\text{-}3}$	1.0	1.3	2.0	A	A
4.10	Low-side overcurrent limitation and shutdown threshold	$20V < V_{VS} < 40V$	2, 12, 15	$I_{Out1\text{-}3}$	–2.0	–1.3	–1.0	A	A
4.11	Overcurrent shutdown delay time			t_{dSd}	10		40	µs	A
4.12	High-side open load detection current	Input register bit 13 (OLD) = low, output off $V_{VS} = 13V$	2, 12, 15	$I_{Out1\text{-}3H}$	–12		–5	mA	A

8. Electrical Characteristics (Continued)

≤ ≤ ≤

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
				$_{outLX}$ / IOL_{outHX}	1.2		3		
4.15	High-side output switch on delay(1),(2)	V_{VS} = 13V R_{Load} = 30Ω		t_{don}			20	µs	A
4.16	Low-side output switch on delay(1),(2)	V_{VS} = 13V R_{Load} = 30Ω		t_{don}			20	µs	A
4.17	High-side output switch off delay(1),(2)	V_{VS} =13V R_{Load} = 30Ω		t_{doff}			20	µs	A
4.18	Low-side output switch off delay(1),(2)	V_{VS} =13V R_{Load} = 30Ω		t_{doff}			3	µs	A
4.19	Dead time between corresponding high-side and low-side switches	V_{VS} =13V R_{Load} = 30Ω		$t_{don} - t_{doff}$	1			µs	A
4.20	Δt_{dPWM} low-side switch(3)	V_{VS} = 13V R_{Load} = 30Ω		$\Delta t_{dPWM} = t_{don} - t_{doff}$			20	µs	A
4.21	Δt_{dPWM} high-side switch(3)	V_{VS} = 13V R_{Load} = 30Ω		$\Delta t_{dPWM} = t_{don} - t_{doff}$	–5		5	µs	A
5	**Logic Inputs DI, CLK, CS, PWM**								
					×				
							×		
				Δ					
6	**Serial Interface – Logic Output DO**								

8. Electrical Characteristics (Continued)

7.5V < V_S < 40V; 4.75V < V_{CC} < 5.25V; INH = High; –40°C ≤ T_j ≤ 200°C; T_a ≤ 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	**Inhibit Input – Timing**								
				dINH			100	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

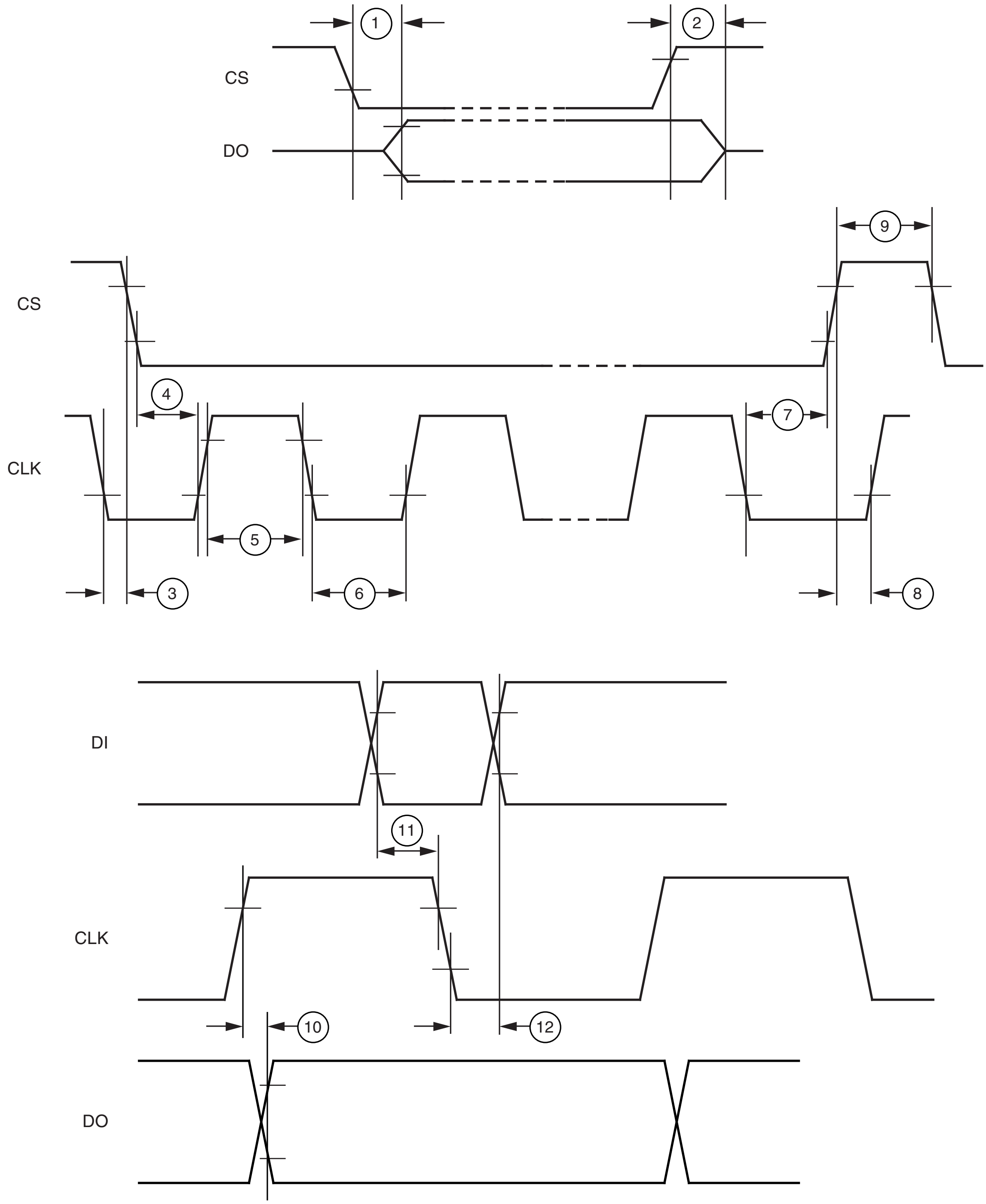
Notes:
1. Delay time between rising edge of input signal at pin CS after data transmission and switch on/off output stages to 90% of final level. Device not in standby for t > 1 ms.
2. Delay time between rising/falling edge of input signal at pin PWM and switch on/off output stages to 90% of final level.
3. Difference between switch-on and switch-off delay time of input signal at pin PWM to output stages in PWM mode.

9. Serial Interface Timing

No.	Parameters	Test Conditions	Pin	Timing Chart No.[1]	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**Serial Interface Timing**									
					ENDO			200	ns	D
8.2	DO disable after CS rising edge	C_{DO} = 100 pF	7	2	t_{DISDO}			200	ns	D
8.3	DO fall time	C_{DO} = 100 pF	7	-	t_{DOf}			100	ns	D
8.4	DO rise time	C_{DO} = 100 pF	7	-	t_{DOr}			100	ns	D
8.5	DO valid time	C_{DO} = 100 pF	7	10	t_{DOVal}			200	ns	D
8.6	CS setup time		3	4	$t_{CSSethl}$	225			ns	D
8.7	CS setup time		3	8	$t_{CSSetlh}$	225			ns	D
8.8	CS high time		3	9	t_{CSh}	500			ns	D
8.9	CLK high time		5	5	t_{CLKh}	225			ns	D
8.10	CLK low time		5	6	t_{CLKl}	225			ns	D
8.11	CLK period time		5	-	t_{CLKp}	500			ns	D
8.12	CLK setup time		5	7	$t_{CLKSethl}$	225			ns	D
8.13	CLK setup time		5	3	$t_{CLKSetlh}$	225			ns	D
8.14	DI setup time		4	11	t_{DIset}	40			ns	D
8.15	DI hold time		4	12	t_{DIHold}	40			ns	D

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

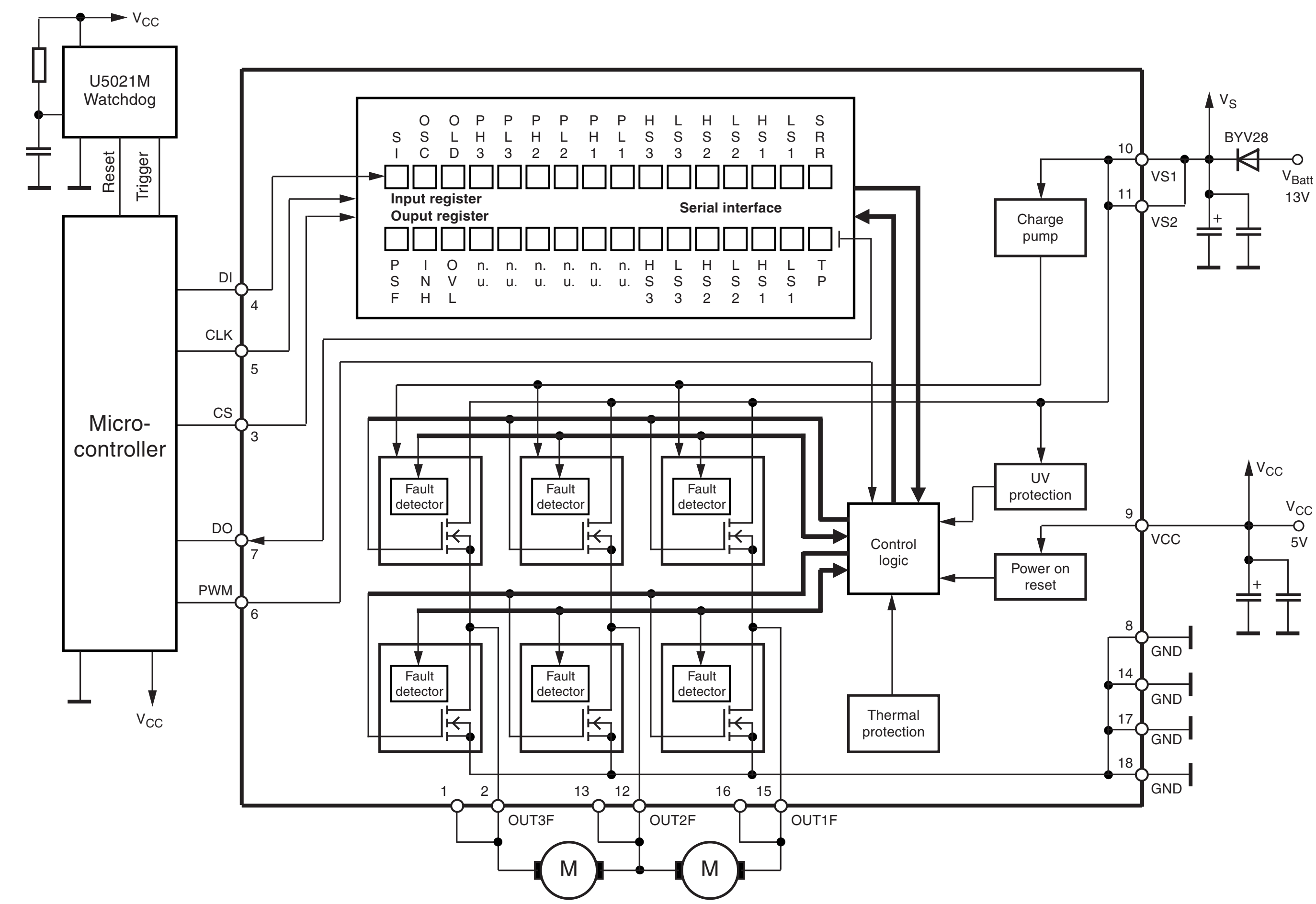
Figure 9-1. Serial Interface Timing with Chart Number



Inputs DI, CLK, CS: High level = 0.7 × V_{CC}, low level = 0.3 × V_{CC}
Output DO: High level = 0.8 × V_{CC}, low level = 0.2 × V_{CC}

10. Application Circuit

Figure 10-1.



10.1 Application Notes

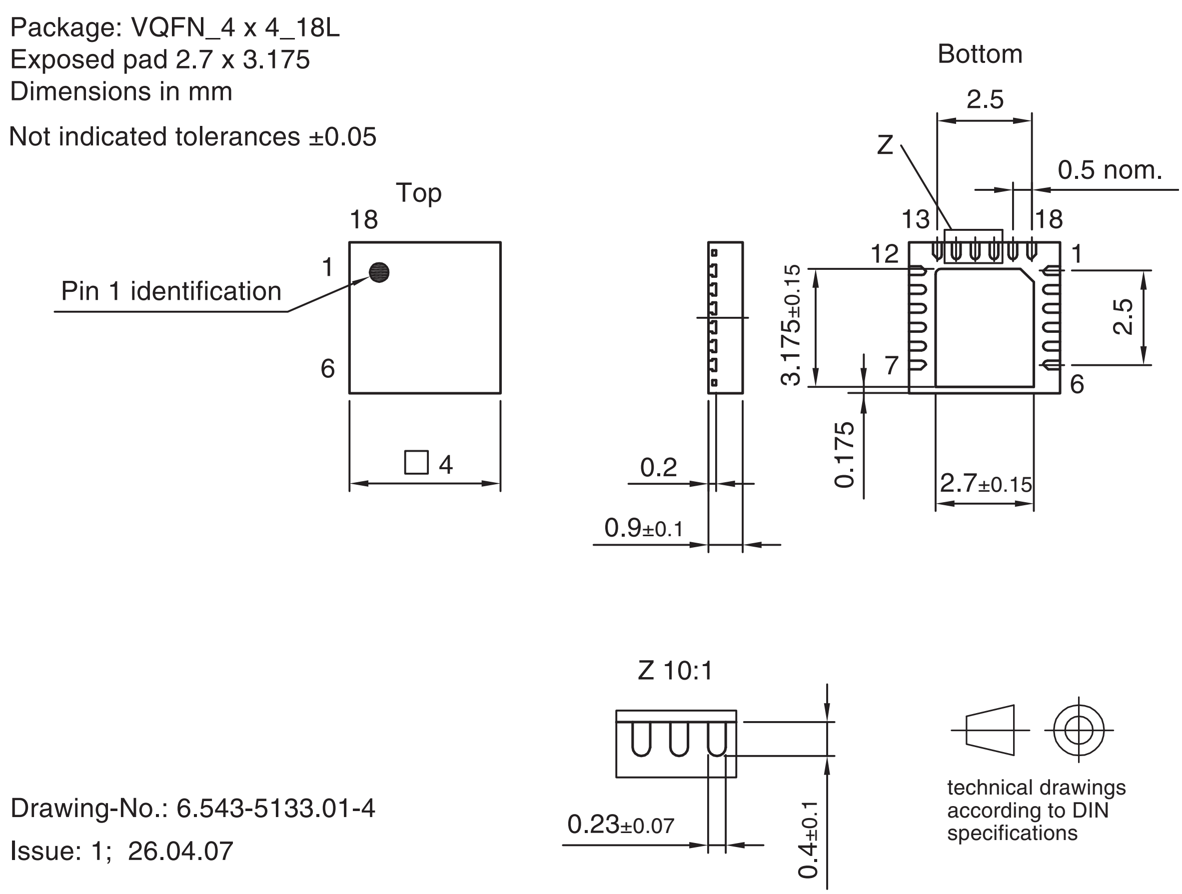
$_{CC}$ and V_S as close as possible to the power supply and GND pins.

- Recommended value for capacitors at V_S:
  - Electrolytic capacitor C > 22 µF in parallel with a ceramic capacitor C = 100 nF. The value for the electrolytic capacitor depends on external loads, conducted interferences, and the reverse conducting current $I_{Out1,2,3}$.
- Recommended value for capacitors at V_{CC}:
  - Electrolytic capacitor C > 10 µF in parallel with a ceramic capacitor C = 100 nF.
- To reduce thermal resistance, place cooling areas on the PCB as close as possible to the GND pins and to the die pad.

11. Ordering Information

Extended Type Number	Package	Remarks
ATA6832-PIQW	QFN18, 4 mm × 4 mm	Taped and reeled, Pb-free

Package Information



13. Revision History

Revision No.	History
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