

## 85mΩ High Function Power Switch

### ■ GENERAL DESCRIPTION

The XC8109 series is a P-channel MOSFET power switch IC with a low ON resistance. A current limit, reverse current prevention (prevents reverse current from  $V_{OUT}$  to  $V_{IN}$ ), soft start, thermal shutdown, and an under voltage lockout (UVLO) are incorporated as protective functions. A flag function monitors the power switch status. The flag output has N-channel open drain structure, and outputs Low level signal while over-current or overheating is detected, or while the reverse current prevention is operated.

A variable current limiting function is integrated, allowing the current limit value to be set, using an external resistor. The voltage level which is fed to CE pin determines the status of XC8109. The logic level of CE pin is selectable between either one of active high or active low.

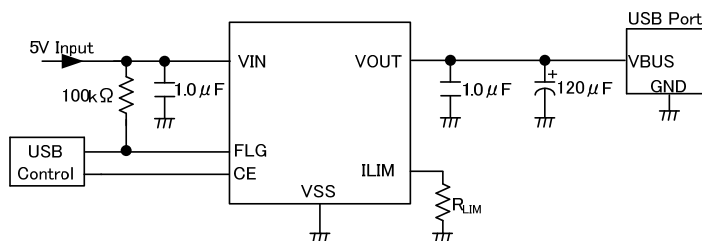
### ■ APPLICATIONS

- Set Top Boxes
- Digital TVs
- PCs
- USB Ports/USB Hubs
- HDMI

### ■ FEATURES

Input Voltage	: 2.5V~5.5V
Maximum Output Current	: 0.9A
ON Resistance	: 85mΩ@ $V_{IN}=5.0V$ (TYP.)
Supply Current	: 40 $\mu A$ @ $V_{IN}=5.0V$
Stand-by Current	: 0.1 $\mu A$ (TYP.)
Flag Delay Time	: 7.5ms (TYP.)
	* At over-current detection
	: 4ms (TYP.)
	* At reverse voltage detection
Protection Circuit	: Reverse Current Prevention 75mA~1.3A (TYP.)
	Thermal Shutdown
	Under Voltage Lockout (UVLO)
	Soft-start
Functions	: Flag Output
	CE Pin Input Logic Selectable
Current Limit Response Time	: 2 $\mu s$ (TYP.) *Reference value
Operating Ambient Temperature	: -40°C~+105°C
Package	: USP-6C
Environmentally Friendly	: EU RoHS Compliant, Pb Free

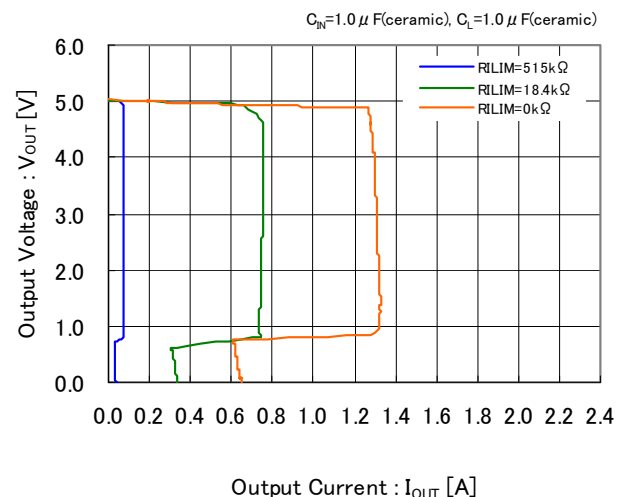
### ■ TYPICAL APPLICATION CIRCUIT



\* The Typical circuit is base on USB high side switch.  
The XC8109 series can accommodate 1  $\mu F$  output capacitor ( $C_L$ ).

### ■ TYPICAL PERFORMANCE CHARACTERISTICS

XC8109xC10ER





## ■ PRODUCT CLASSIFICATION

### ● Ordering Information

XC8109①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	CE Logic	A	Refer to Selection Guide
		B	
②	Protection Circuits Type	C	
		D	
③④	Maximum Output Current	10	0.9A (* Adjustable current limit range:75mA~1300mA)
⑤⑥-⑦ (*1)	Package (Order Unit)	ER-G	USP-6C (3,000pcs/Reel)

(\*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

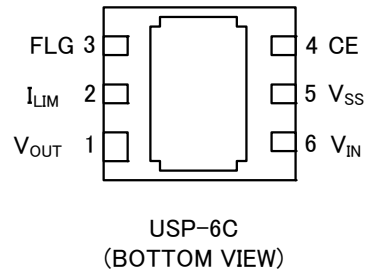
### ● Selection Guide

TYPE	CE LOGIC SELECTABLE	SOFT-START	CURRENT LIMIT ADJUSTABLE
AC	Active High	Yes	Yes
AD	Active High	Yes	Yes
BC	Active Low	Yes	Yes
BD	Active Low	Yes	Yes

TYPE	UVLO	FLG OUTPUT	REVERSE CURRENT PREVENTION
AC	Yes	Yes	Yes
AD	Yes	Yes	Yes
BC	Yes	Yes	Yes
BD	Yes	Yes	Yes

TYPE	THERMAL SHUT DOWN	LATCH PROTECTION
AC	Yes	No
AD	Yes	Yes
BC	Yes	No
BD	Yes	Yes

## ■ PIN CONFIGURATION



\* The dissipation pad for the USP-6C packages should be solder-plated for mounting strength and heat dissipation. Please refer to the reference mount pattern and metal masking. The dissipation pad should be connected to the  $V_{SS}$  (No. 5) pin.

## ■ PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
USP-6C		
1	$V_{OUT}$	Output
2	$I_{LIM}$	Current Limit Adjustment
3	FLG	Fault Report
4	CE	ON/OFF Control
5	$V_{SS}$	Ground
6	$V_{IN}$	Power Input

## ■ FUNCTION

TYPE	PIN NAME	SIGNAL	STATUS
A	CE	H	Active
		L	Stand-by
		OPEN	Undefined State (*1)
B		H	Stand-by
		L	Active
		OPEN	Undefined State (*1)

\* Avoid leaving the CE pin open; set to any fixed voltage.

## ■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V <sub>IN</sub>	-0.3~+6.0	V
Output Voltage		V <sub>OUT</sub>	-0.3~+6.0	V
Output Current		I <sub>OUT</sub>	1.7	A
CE Input Voltage		V <sub>CE</sub>	-0.3~+6.0	V
FLG Pin Voltage		V <sub>FLG</sub>	-0.3~+6.0	V
FLG Pin Current		I <sub>FLG</sub>	15	mA
I <sub>LIM</sub> Pin Voltage		V <sub>LIM</sub>	-0.3~+6.0	V
I <sub>LIM</sub> Pin Current		I <sub>LIM</sub>	±1	mA
Power Dissipation	USP-6C	Pd	120	mW
			1000 (40mm x 40mm Standard board) <sup>(*)2)</sup>	
			1250 (JEDEC board) <sup>(*)2)</sup>	
Operating Ambient Temperature		T <sub>opr</sub>	-40~+105	°C
Storage Temperature		T <sub>stg</sub>	-55~+125	°C

\* All voltages are described based on the V<sub>SS</sub>.

<sup>(\*)1)</sup> Use with I<sub>OUT</sub> less than Pd/(V<sub>IN</sub>-V<sub>OUT</sub>).

<sup>(\*)2)</sup> This is a reference data taken by using the test board. Please see the power dissipation page for the mounting condition.

## ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V <sub>IN</sub>	-	2.5	-	5.5	V	①
On Resistance	R <sub>ON</sub>	V <sub>IN</sub> =3.3V, I <sub>OUT</sub> =1.0A	-	100	110	mΩ	①
		V <sub>IN</sub> =5.0V, I <sub>OUT</sub> =1.0A	-	85	104	mΩ	
Supply Current	I <sub>SS</sub>	V <sub>OUT</sub> =OPEN	-	40	75	μA	②
Stand-by Current	I <sub>STBY</sub>	V <sub>IN</sub> =5.5V, V <sub>OUT</sub> =OPEN V <sub>CE</sub> =V <sub>SS</sub> (XC8109A series) V <sub>CE</sub> =V <sub>IN</sub> (XC8109B series)	-	0.01	1.0	μA	②
Switch Leakage Current	I <sub>LEAK</sub>	V <sub>IN</sub> =5.5V, V <sub>OUT</sub> =0V V <sub>CE</sub> =V <sub>SS</sub> (XC8109A series) V <sub>CE</sub> =V <sub>IN</sub> (XC8109B series)	-	0.01	1.0	μA	②
Current Limit	I <sub>LIMIT</sub>	V <sub>OUT</sub> =V <sub>IN</sub> -0.3V I <sub>LIMIT</sub> shorted to V <sub>SS</sub>	1.170	1.300	1.430	A	①
		V <sub>OUT</sub> =V <sub>IN</sub> -0.3V R <sub>LIMIT</sub> =18.4kΩ	0.621	0.730	0.840		
Short-Circuit Current	I <sub>SHORT</sub>	V <sub>OUT</sub> =0V I <sub>LIMIT</sub> shorted to V <sub>SS</sub>	-	0.650	-	A	①
		V <sub>OUT</sub> =0V R <sub>LIMIT</sub> =18.4kΩ	-	0.365	-		
Current Limit Circuit Response Time <sup>(*)</sup>	t <sub>CLR</sub>	V <sub>IN</sub> =5.0V, V <sub>OUT</sub> : OPEN→0V Measure from V <sub>OUT</sub> =0V to when current falls below a certain I <sub>LIMIT</sub> value	-	2.0	-	μs	①
CE "H" Level Voltage	V <sub>CEH</sub>	V <sub>IN</sub> =5.5V, XC8109A series	1.5	-	5.5	V	①
		V <sub>IN</sub> =5.5V, XC8109B series	-	-	0.8		
CE "L" Level Voltage	V <sub>CEL</sub>	V <sub>IN</sub> =5.5V, XC8109A series	-	-	0.8	V	①
		V <sub>IN</sub> =5.5V, XC8109B series	1.5	-	5.5		
CE "H" Level Current	I <sub>CEH</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =5.5V	-0.1	-	0.1	μA	①
CE "L" Level Current	I <sub>CEL</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =0V	-0.1	-	0.1	μA	①
UVLO Detected Voltage	V <sub>UVLOD</sub>	V <sub>IN</sub> : 2.2V→1.7V	1.8	1.9	2.0	V	①
UVLO Released Voltage	V <sub>UVLOR</sub>	V <sub>IN</sub> : 1.7V→2.2V	1.9	2.0	2.1	V	①
UVLO Hysteresis	V <sub>UHYS</sub>	-	-	0.1	-	V	①

**NOTE:**

Unless otherwise stated, V<sub>IN</sub>=5.0V, I<sub>OUT</sub>=1mA, I<sub>LIMIT</sub>=V<sub>SS</sub>, V<sub>CE</sub>=V<sub>IN</sub> (XC8109A series) or V<sub>CE</sub>=V<sub>SS</sub> (XC8109B series)

<sup>(\*)</sup> Design reference value. This parameter is provided only for reference.

## ■ ELECTRICAL CHARACTERISTICS (Continued)

Ta=25°C

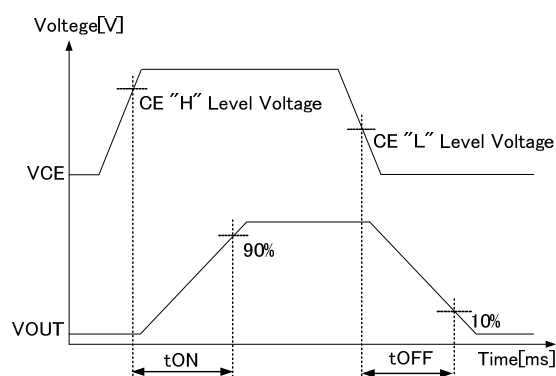
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
turn-on time	t <sub>ON</sub>	R <sub>LOAD</sub> =10Ω, V <sub>CE</sub> =0V→2.2V	-	0.60	1.00	ms	①
turn-off time	t <sub>OFF</sub>	R <sub>LOAD</sub> =10Ω, V <sub>CE</sub> =2.2V→0V	-	0.08	0.13	ms	①
FLG output FET On-resistance	R <sub>FLG</sub>	I <sub>FLG</sub> =10mA, V <sub>OUT</sub> =5.5V	-	15	20	Ω	③
FLG output FET Leakage Current	I <sub>FOFF</sub>	V <sub>IN</sub> =5.5V, V <sub>FLG</sub> =5.5V, V <sub>OUT</sub> =OPEN	-	0.01	0.1	μA	③
FLG delay time	t <sub>FD1</sub>	over-current condition	6.5	7.5	8.5	ms	①
	t <sub>FD2</sub>	reverse-voltage condition	2.7	4.0	4.7	ms	①
Reverse Current	I <sub>REV</sub>	V <sub>IN</sub> =0V, V <sub>OUT</sub> =5.5V V <sub>CE</sub> =5.0V (XC8109A series) V <sub>CE</sub> =V <sub>SS</sub> (XC8109B series)	-	0.1	1.0	μA	①
Reverse Current Prevention Detect Voltage	V <sub>REV_D</sub>	V <sub>IN</sub> : 5.0V→4.7V V <sub>OUT</sub> =5.0V	-	140	-	mV	①
Thermal Shutdown Detect Temperature	T <sub>TSD</sub>	Junction Temperature	-	150	-	°C	①
Thermal Shutdown Release Temperature	T <sub>TSR</sub>	Junction Temperature	-	130	-	°C	①
Thermal Shutdown Hysteresis Width	T <sub>HYS</sub>	Junction Temperature	-	20	-	°C	①

NOTE:

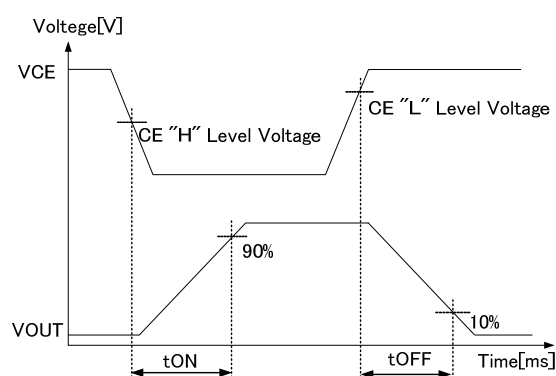
Unless otherwise stated, V<sub>IN</sub>=5.0V, I<sub>OUT</sub>=1mA, I<sub>LIM</sub>=V<sub>SS</sub>, V<sub>CE</sub>=V<sub>IN</sub> (XC8109A series) or V<sub>CE</sub>=V<sub>SS</sub> (XC8109B series)

## ■ TIMING CHART

● turn-on time, turn-off time



XC8109 Series, Type A

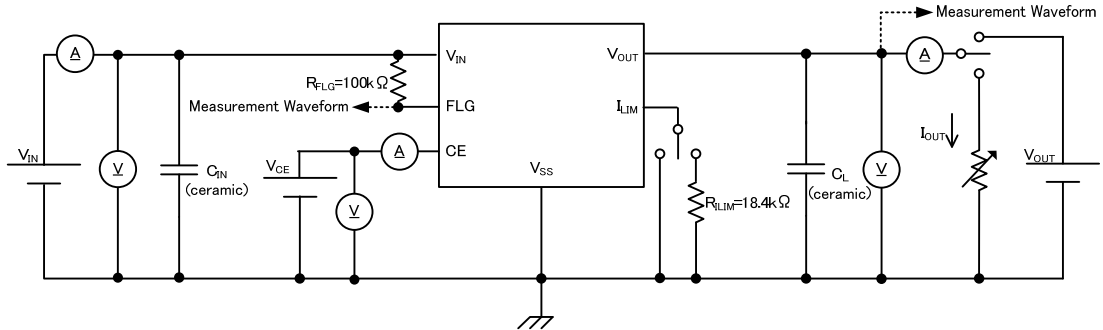


XC8109 Series, Type B

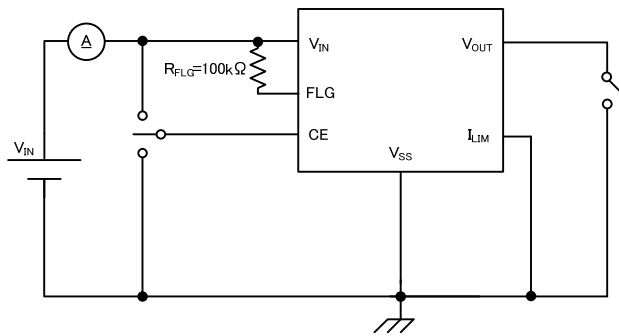
## TEST CIRCUITS

$C_{IN}=1.0\ \mu F$ ,  $C_L=1.0\ \mu F$

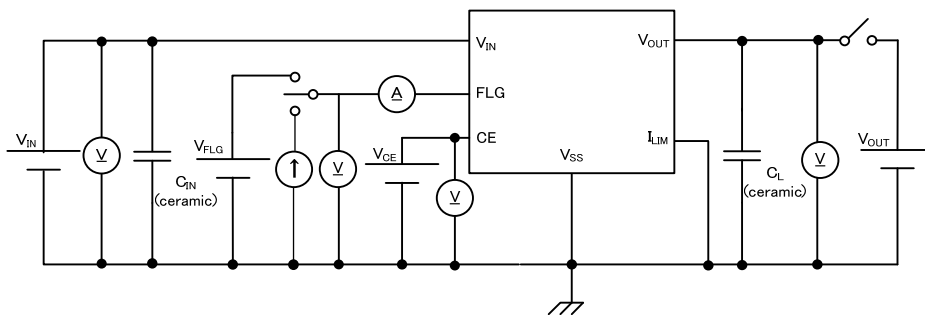
### 1) CIRCUIT①



### 2) CIRCUIT②



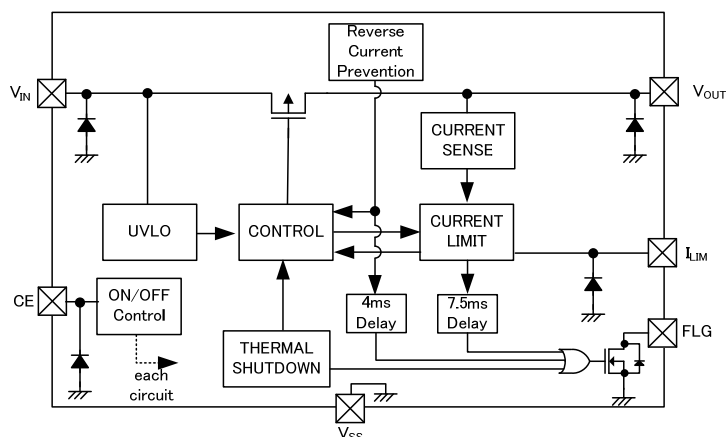
### 3) CIRCUIT③





## ■ OPERATIONAL EXPLANATION

The XC8109 series is a P-channel MOSFET power switch IC. The XC8109 series consists of a CE circuit, UVLO circuit, thermal shutdown circuit, current limiter circuit, reverse current prevention circuit, control block and others. The gate voltage of the power switch transistor is controlled with control block. The current limiter circuit and reverse current prevention circuit will operate based on the output voltage and output current. (See the BLOCK DIAGRAM below)



BLOCK DIAGRAM (XC8109 Series)

### <CE Pin>

The voltage level which is fed to CE pin controls the status of this IC. If either “H” level or “L” level which is defined as the electrical specification is fed to CE pin, then XC8109 can operate in standard manner. However, if the middle voltage which is neither “H” level nor “L” level is fed to CE pin, the consumption current will increase due to the shoot-through current at internal circuits. Also if CE pin is open, the status of XC8109 cannot be fixed and the behavior will be unstable.

### <Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function is built in. When the internal junction temperature reaches the temperature limit, the thermal shutdown circuit operates and the power switch transistor will turn OFF. The IC resumes its operation when the thermal shutdown function is released and the IC’s operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature. When the thermal shutdown circuit detects higher junction temperature than the detect temperature, the voltage level of FLG pin is low level. When the thermal shutdown circuit detects lower junction temperature than the release temperature, the thermal shutdown function is released and the voltage level of FLG pin is high level.

### <Under Voltage Lockout (UVLO) >

When the  $V_{IN}$  pin voltage goes down to lower voltage than UVLO detected voltage, the power switch transistor turns OFF by UVLO function in order to prevent false output caused by unstable operation of the internal circuitry. When the  $V_{IN}$  pin voltage goes up to higher voltage than UVLO released voltage, the UVLO function is released and the power switch transistor can turn ON.

### <Soft-start Function>

The soft-start circuit can reduce the in-rush current charged on the output capacitor when IC starts up. Additionally, due to the reduction of the in-rush current, the circuit can reduce the fluctuation of the input voltage as well. The soft-start time is optimized internally and defined as turn-on time. (TYP: 0.6ms)

## OPERATIONAL EXPLANATION (Continued)

### <Current limiter, short-circuit protection>

When the output current reaches the current limit value, the constant current limit circuit activates and as a result, the output voltage goes down.

If the short circuit comes at the  $V_{OUT}$  pin, the output current is limited to the current which is specified as the short-circuit current value. In over-current states, after output voltage drops and the situation is kept for 7.5ms (TYP.), the FLG pin changes to Low level output.

Two types are available for the current limiter circuit: an auto recovery type (product type C) and a latch off type (product type D). After the current limiter circuit activates and the FLG pin outputs low level, the operation is different between these two types.

The auto recovery type continuously limits the output current by the current limit value. In over-current states, after output voltage returns to normal and the situation is kept for 7.5ms (TYP.), the voltage of FLG pin goes up "H" level again.

The latch off type turns off the power switch transistor after the FLG pin outputs Low level. The off state is maintained regardless of whether the over-current state is released.

Latch operation is released by turning off the IC with the CE pin signal and then restarting, or by lowering the input voltage below the UVLO detected voltage once and after that raising it higher than UVLO released voltage.

### <Current limit external adjustment function>

By connecting a resistor to the current limit external adjustment pin ( $I_{LIM}$  pin), the current limit can be set to any value. By the following equations, the current limit value can be set to any value within a range of 75mA to 1300mA. When the  $I_{LIM}$  pin is open, the switch transistor is forcibly turned off.

(In the case of  $I_{LIMIT(T)} \geq 500\text{mA}$ .)

$$\text{equation 1. } R_{LIM}(\text{k}\Omega) = 32164 / I_{LIMIT(T)}(\text{mA}) - 25.71(\text{k}\Omega)$$

(In the case of  $I_{LIMIT(T)} < 500\text{mA}$ .)

$$\text{equation 2. } R_{LIM}(\text{k}\Omega) = 130170 / I_{LIMIT(T)}(\text{mA})^{1.2814}(\text{k}\Omega)$$

$R_{LIM}$ : External resistance value     $I_{LIMIT(T)}$ : Current limit set value

Table1. Current limit set value

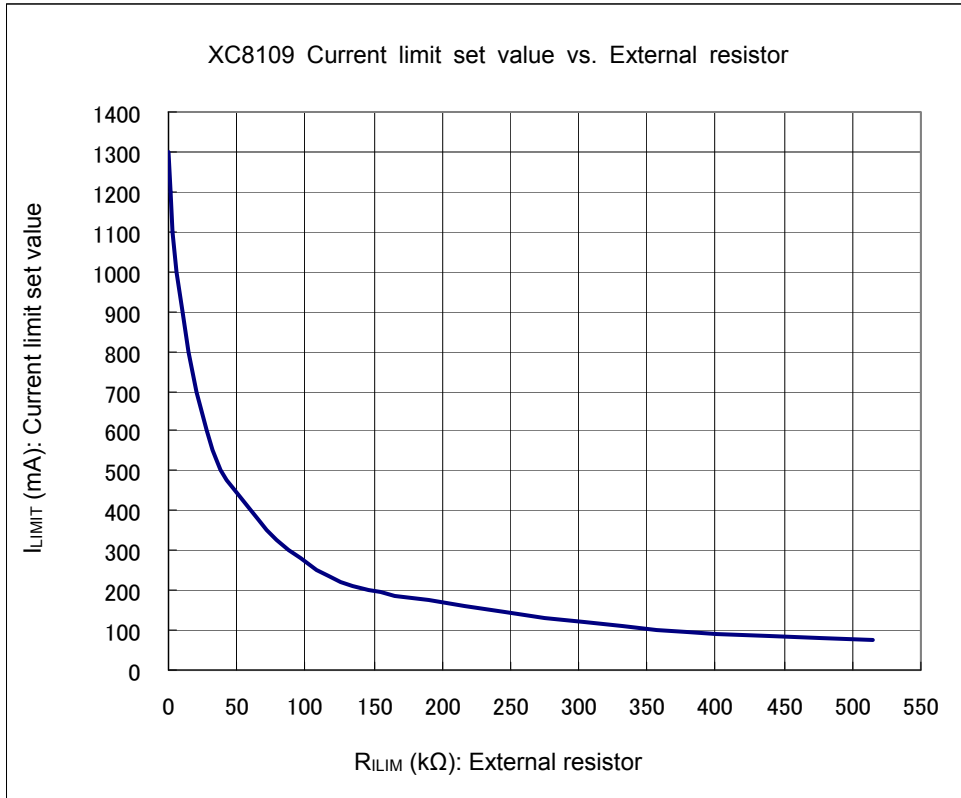
$I_{LIMIT(T)}$ (mA)	$R_{LIM}$ (k $\Omega$ )	E96 External resistance value (k $\Omega$ )	Current limit value when use E96 external resistance (mA) <sup>(*)</sup>		
			MIN.	TYP.	MAX.
75	515	511	49	75	102
100	356	357	69	100	131
200	147	147	156	200	243
300	87.2	86.6	241	302	362
400	60.3	60.4	314	399	485
500	38.6	38.3	427	503	578
600	27.9	28.0	509	599	689
700	20.2	20.0	598	704	809
800	14.5	14.7	716	796	876
900	10.0	10.0	811	901	991
1000	6.46	6.49	899	999	1099
1100	3.53	3.57	989	1099	1208
1200	1.09	1.10	1080	1200	1320
1300	$I_{LIM}$ shorted to $V_{SS}$		1170	1300	1430

<sup>(\*)</sup> MIN. value and MAX. value are reference values.

## OPERATIONAL EXPLANATION (Continued)

<Current limit external adjustment function> (Continued)

Fig1. Current limit set value



## OPERATIONAL EXPLANATION (Continued)

<Current limit external adjustment function> (Continued)

The TYP value of dropout Voltage which is the voltage difference between  $V_{IN}$  and  $V_{OUT}$  is defined by the equation 3 using output current ( $I_{OUT}$ ).

$$\text{equation 3. } V_{dif}(mV) = I_{OUT}(mA) \times 0.085(\Omega)$$

The maximum value of dropout voltage has the influence of the setting of a current limit circuit. (Refer to Table 2)

**【Example】** In the case of  $I_{LIMIT(T)}=500mA$ , When output current is 200mA, dropout voltage MAX. value is 22mV.

Table2. Dropout voltage MAX. value (\*) unit: (mV)

Output Current: $I_{OUT}$	Dropout voltage MAX. value						
	Current limit set value: $I_{LIMIT(T)}$						
	75mA	100mA	200mA	300mA	400mA	500mA	600mA
10mA	4	3	1	1	1	1	1
30mA	15	10	5	4	3	3	3
50mA	41	24	9	6	5	5	5
70mA	-	49	14	10	8	7	7
100mA	-	-	28	15	12	10	10
150mA	-	-	71	29	20	15	15
200mA	-	-	-	55	33	22	20
250mA	-	-	-	112	58	32	26
300mA	-	-	-	-	100	46	35
400mA	-	-	-	-	-	105	67
500mA	-	-	-	-	-	-	143

unit: (mV)

Output Current: $I_{OUT}$	Dropout voltage MAX. value						
	Current limit set value: $I_{LIMIT(T)}$						
	700mA	800mA	900mA	1000mA	1100mA	1200mA	1300mA
10mA	1	1	1	1	1	1	1
30mA	3	3	3	3	3	3	3
50mA	5	5	5	5	5	5	5
70mA	7	7	7	7	7	7	7
100mA	10	10	10	10	10	10	10
150mA	15	15	15	15	15	15	15
200mA	20	20	20	20	20	20	20
250mA	26	26	26	26	26	26	26
300mA	30	30	30	30	30	30	30
400mA	48	41	41	41	41	41	41
500mA	85	60	51	51	51	51	51
600mA	167	100	75	61	61	61	61
700mA	-	183	122	85	71	71	71
800mA	-	-	214	132	97	82	81
900mA	-	-	-	223	144	107	92

(\*) MAX. value is reference value.

## ■ OPERATIONAL EXPLANATION (Continued)

### <Reverse current prevention>

An internal circuit is built in that prevents reverse current from the V<sub>OUT</sub> pin to the V<sub>IN</sub> pin.

When the difference between input voltage and V<sub>OUT</sub> pin voltage is higher than the detect voltage set internally, the reverse current prevention circuit activates, and the power switch transistor turns off, then the reverse current from the V<sub>OUT</sub> pin to the V<sub>IN</sub> pin is reduced to 0.1 μA (TYP.).

If the reverse-voltage state lasts for 4ms (TYP.), the FLG pin changes to Low level output.

Two types are available for the reverse current prevention circuit: the auto recovery type (product type C) and the latch off type (product type D). After the reverse current prevention circuit activates and the FLG pin outputs low level, the operation is different between these two types.

On the auto recovery type, when the output voltage drops below the input voltage, the reverse current prevention circuit stops immediately, and the power switch transistor turns on again. If the output voltage remains lower than the input voltage for 4ms (TYP.), the FLG pin returns to High level output.

On the latch off type, the power switch transistor remains in the off state even if the reverse voltage state is released.

### <Flag function>

The flag circuit is built in which monitors the state of the power switch.

The FLG pin outputs Low level when the reverse current prevention function is operating. A resistance of 10kΩ to 100kΩ is recommended for the FLG pin pull-up resistance.

#### Auto recovery type (product type C)

Protective function	FLG pin Low level output	Return to FLG pin High level output
Current limiter	In over-current states, after output voltage drops and the situation is kept for 7.5ms (TYP.).	In over-current states, after output voltage returns to normal and the situation is kept for 7.5ms (TYP.).
Reverse current prevention	4.0ms after reverse voltage detection	4.0ms after reverse voltage release
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released

#### Latch off type (product type D)

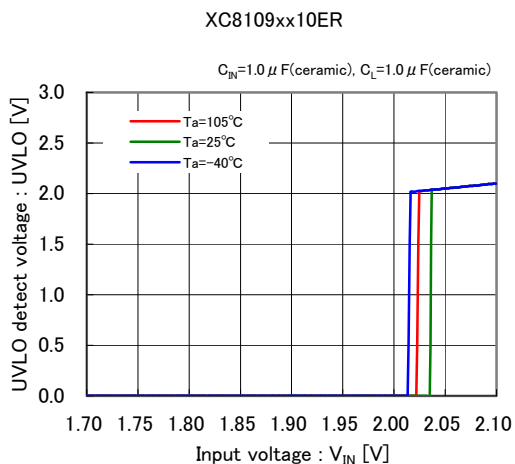
Protective function	FLG pin Low level output	Return to FLG pin High level output
Current limiter	In over-current states, after output voltage drops and the situation is kept for 7.5ms (TYP.).	When latch operation is released
Reverse current prevention	4.0ms after reverse voltage detection	When latch operation is released
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released

## ■ NOTES ON USE

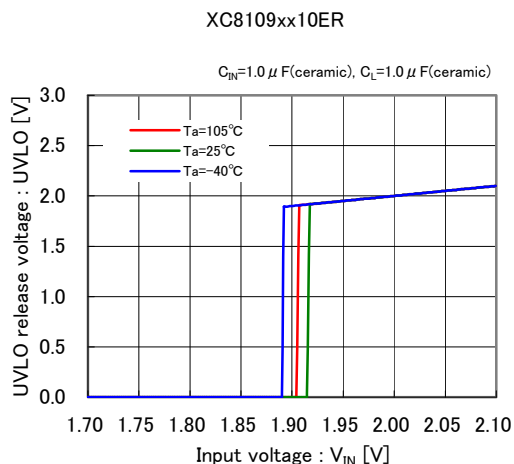
1. For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.
2. Where wiring impedance is high, operations may become unstable due to noise depending on output current.  
Please keep the resistance low between  $V_{IN}$  and  $V_{SS}$  wiring in particular.
3. Please place the input capacitor ( $C_{IN}$ ) and the output capacitor ( $C_L$ ) as close to the IC as possible.  
For the input or output capacitor, a capacitance of  $1.0 \mu F$  or higher is recommended.
4. When the voltage which is higher than the maximum input voltage is fed to the  $V_{IN}$  pin, and  $V_{OUT}$  is shorted to the  $V_{SS}$  level, in this case the short circuit may cause a fatal impact to operation for the IC. Please use within the operational voltage range.
5. The current limit value can be adjusted by external resistor ( $R_{LIM}$ ). The characteristic of the resistor influence the current limit value, please choose the resistor with small tolerance and temperature coefficient.
6. 80% of current limit set value is the recommended value of maximum output current.
7. Torex places an importance on improving our products and its reliability.  
However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

## TYPICAL PERFORMANCE CHARACTERISTICS

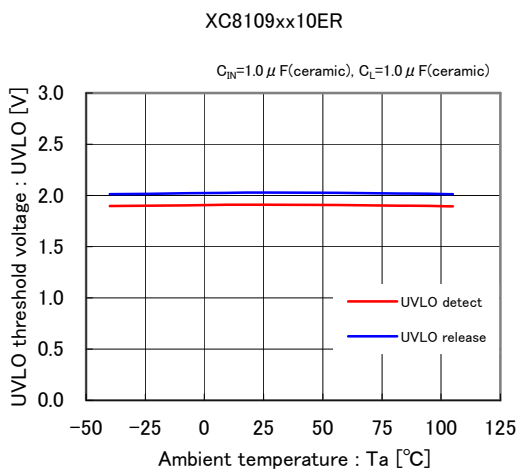
(1) UVLO detect voltage vs. Input voltage



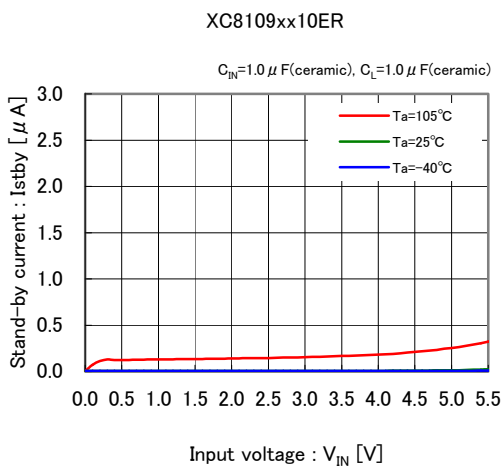
(2) UVLO release voltage vs. Input voltage



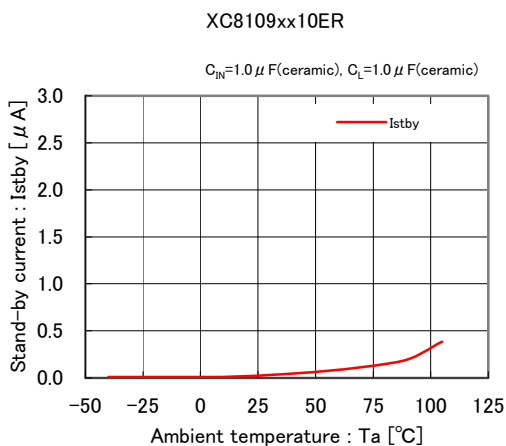
(3) UVLO threshold voltage vs. Ambient temperature



(4) Stand-by current vs. Input voltage

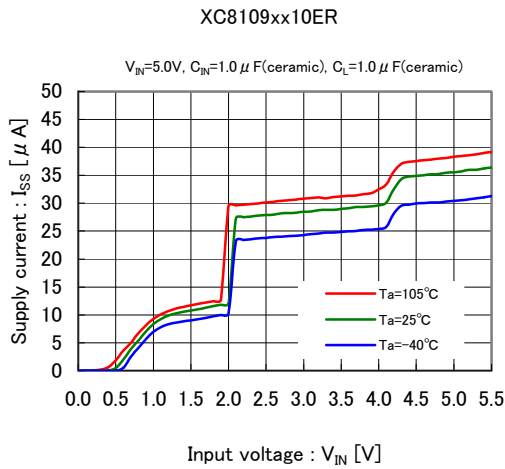


(5) Stand-by current vs. Ambient temperature

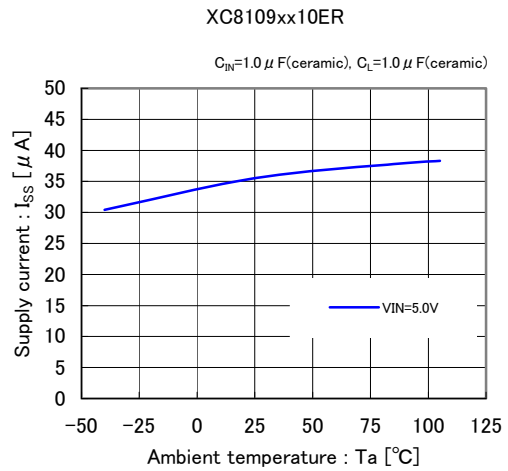


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

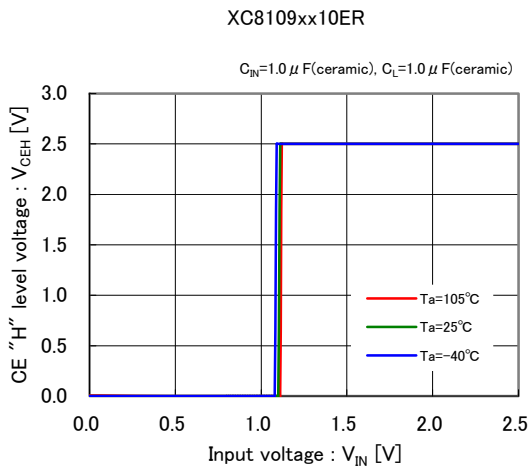
(6) Supply current vs. Input voltage (sweep up)



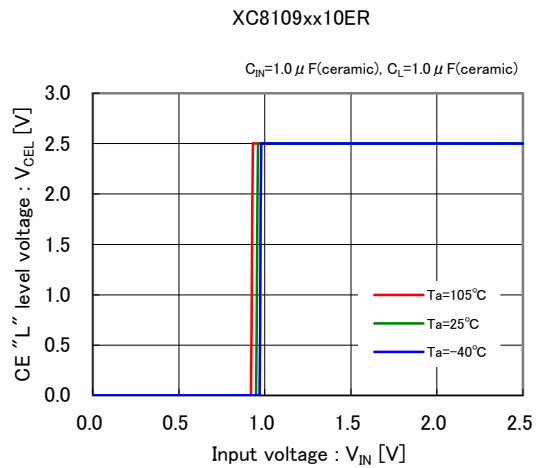
(7) Supply current vs. Ambient temperature



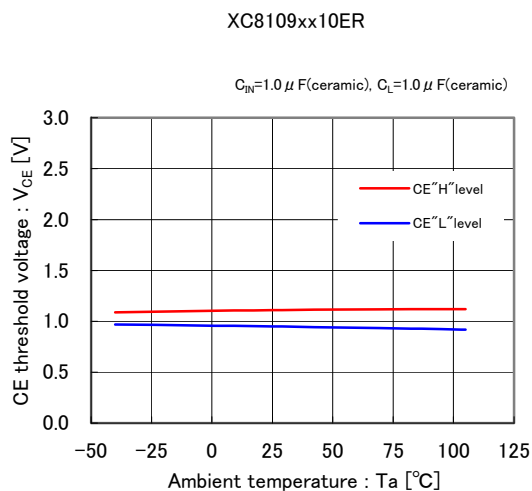
(8) CE "H" level voltage vs. Input voltage



(9) CE "L" level voltage vs. Input voltage



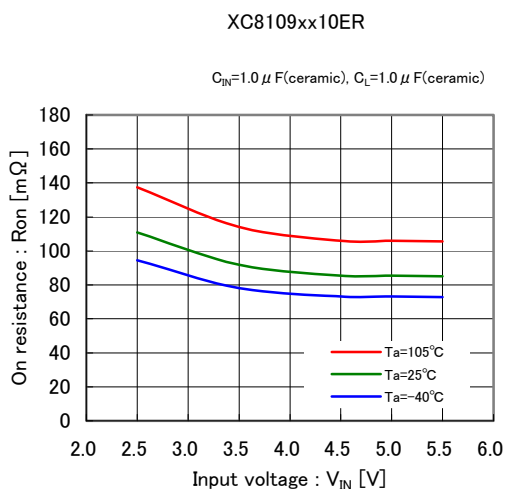
(10) CE threshold voltage vs. Ambient temperature



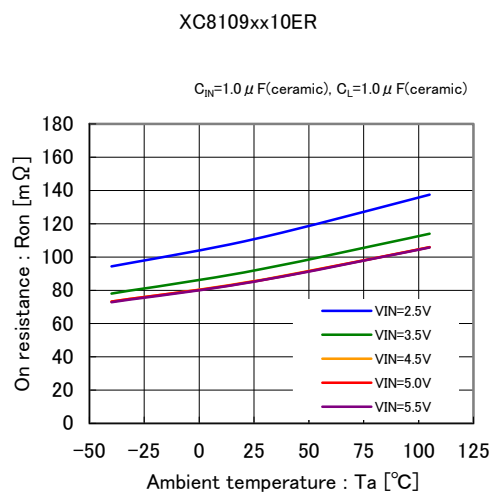


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

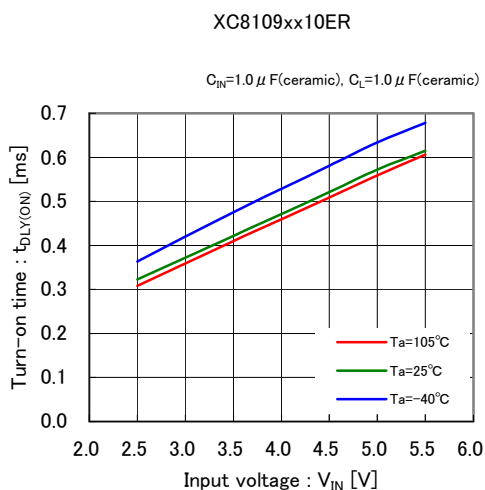
(11) On resistance vs. Input voltage



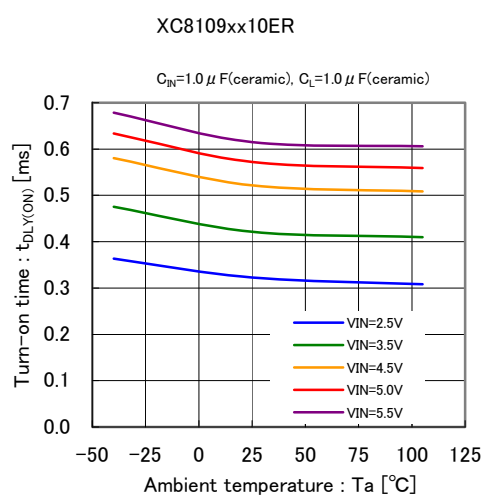
(12) On resistance vs. Ambient temperature



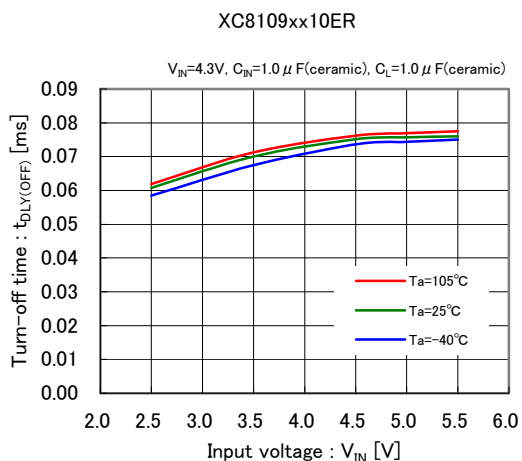
(13) Turn-on time vs. Input voltage



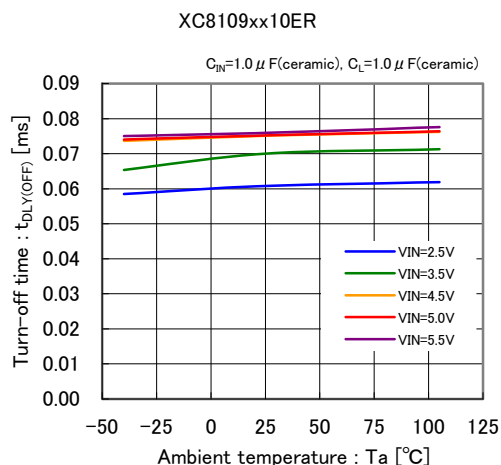
(14) Turn-on time vs. Ambient temperature



(15) Turn-off time vs. Input voltage

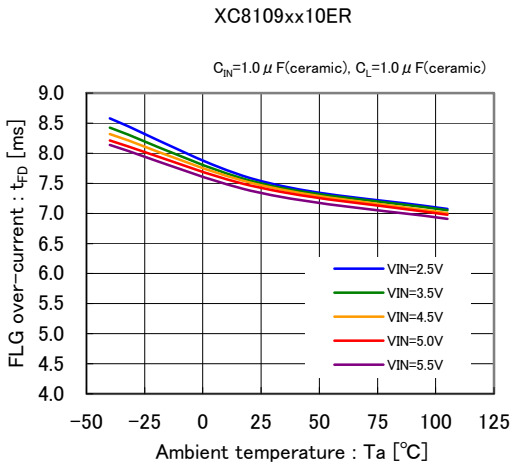


(16) Turn-off time vs. Ambient temperature

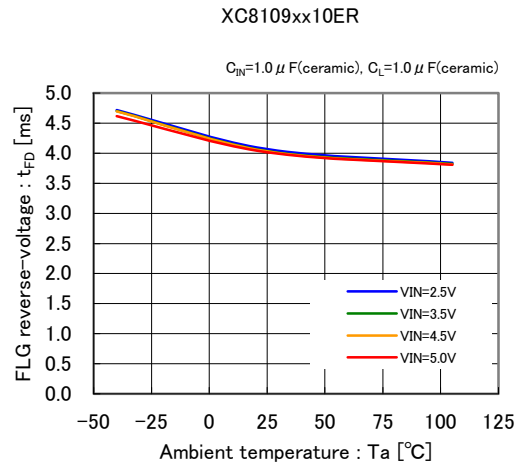


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

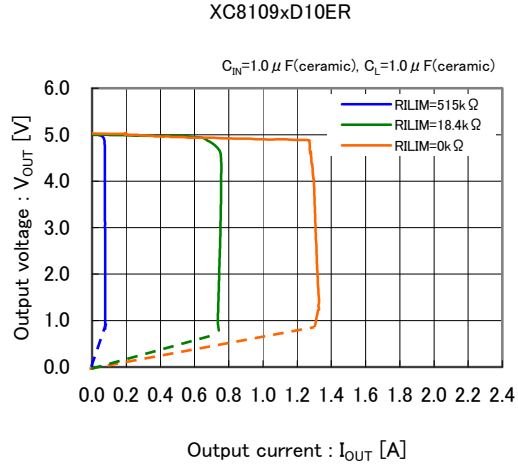
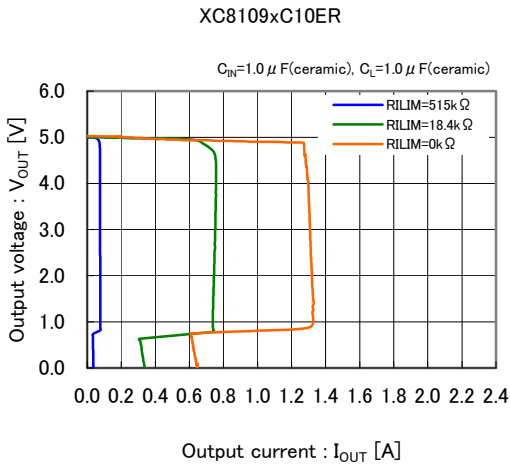
(17) FLG delay time over-current vs. Ambient temperature



(18) FLG delay time reverse-voltage vs. Ambient temperature

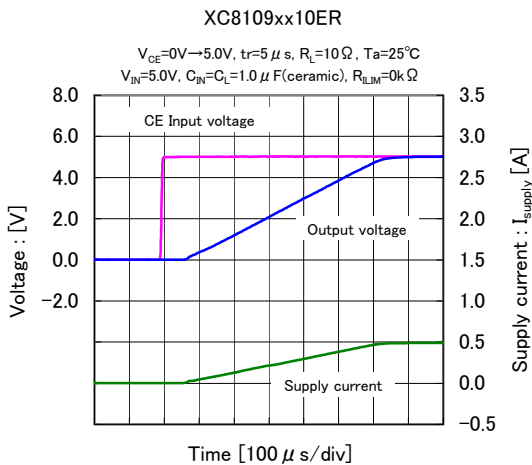


(19) Output voltage vs. Output current

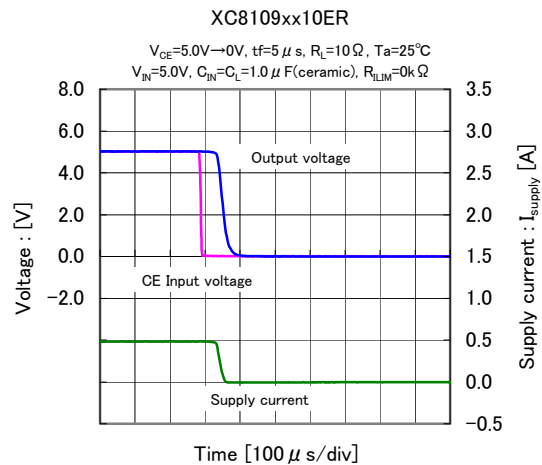


In over-current states, after output voltage drops and the lapse of 7.5ms, the latch off type turns off the power switch transistor.

(20) Turn-on delay vs. Rise time ( $C_L=1.0\ \mu\text{F}$ )

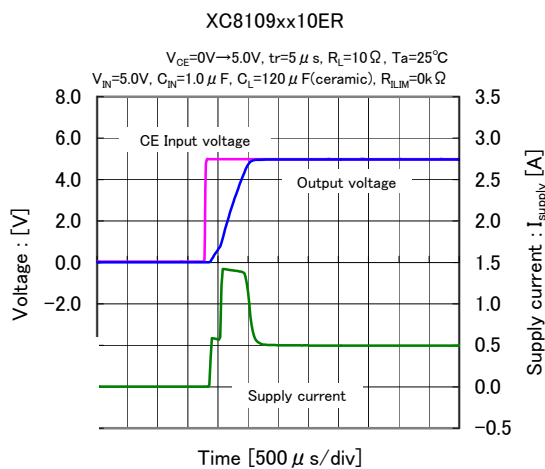


(21) Turn-off delay vs. Fall time ( $C_L=1.0\ \mu\text{F}$ )

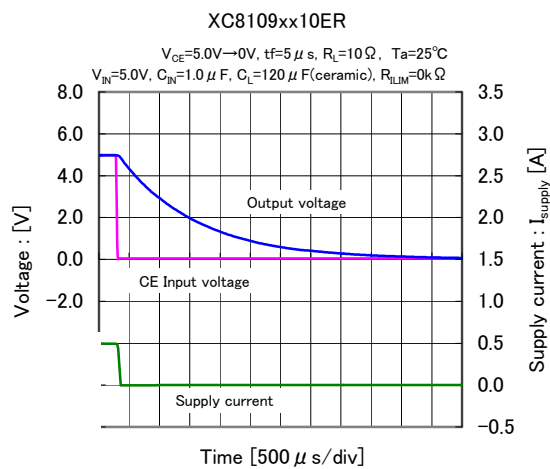


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

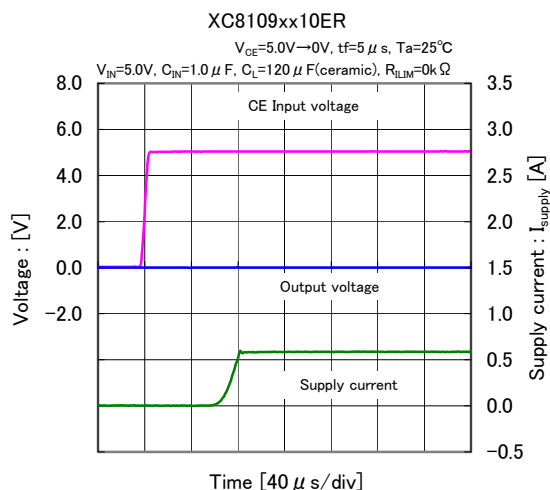
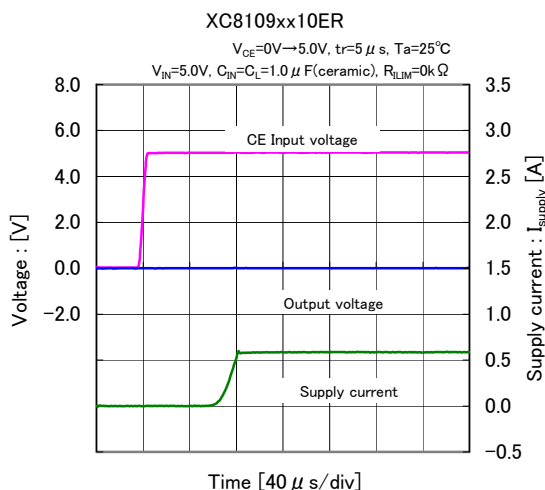
(22) Turn-on delay vs. Rise time ( $C_L=120\ \mu\text{F}$ )



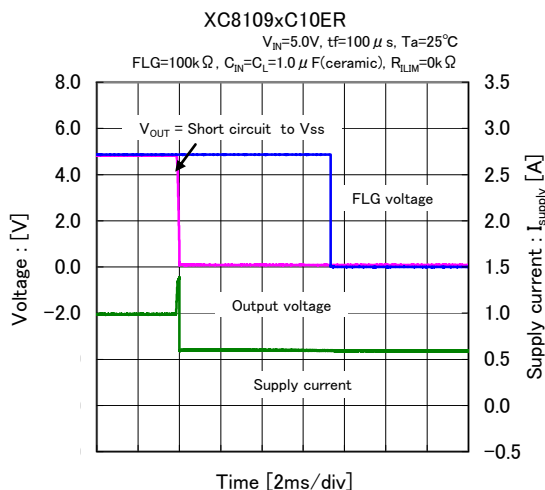
(23) Turn-off delay vs. Fall time ( $C_L=120\ \mu\text{F}$ )



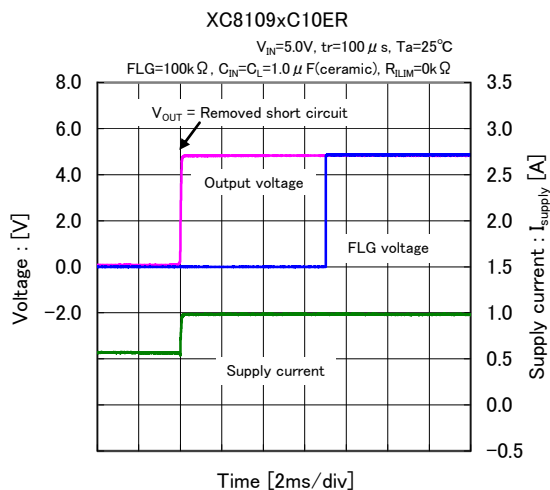
(24) Short circuit current, Device enabled into short



(25) Short-circuit transient response  
( $V_{OUT}=5.0\ \Omega \rightarrow \text{short}$ ,  $C_L=1.0\ \mu\text{F}$ )

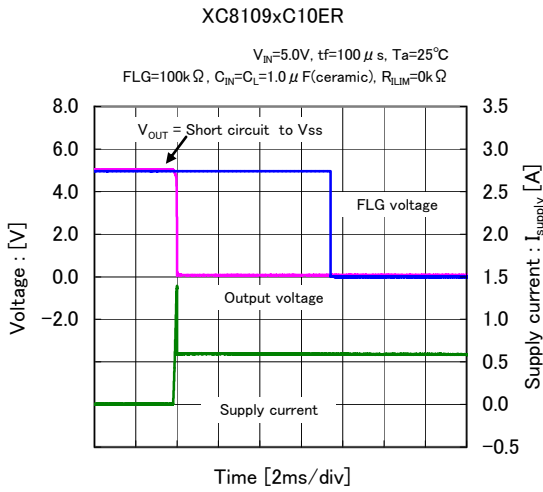


(26) Short-circuit transient response  
( $V_{OUT}=\text{short} \rightarrow 5.0\ \Omega$ ,  $C_L=1.0\ \mu\text{F}$ )

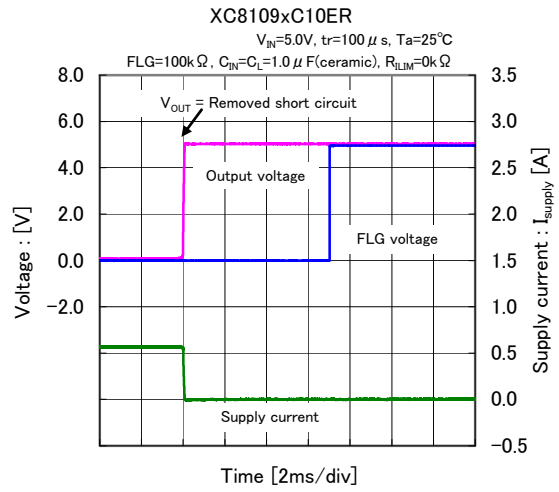


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

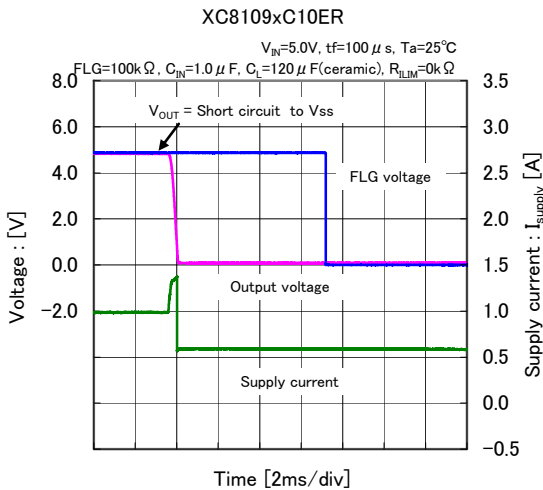
(27) Short-circuit transient response  
( $V_{OUT}$ =open $\rightarrow$ short,  $C_L=1.0\mu F$ )



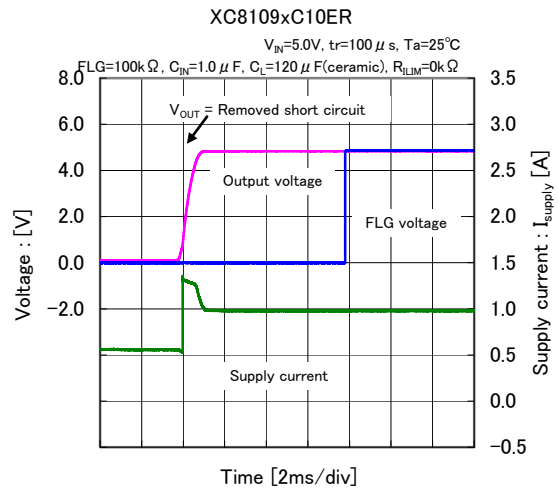
(28) Short-circuit transient response  
( $V_{OUT}$ =short $\rightarrow$ open,  $C_L=1.0\mu F$ )



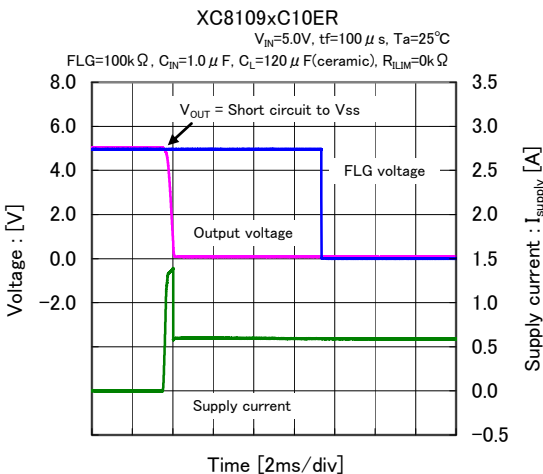
(29) Short-circuit transient response  
( $V_{OUT}=5.0\Omega \rightarrow$ short,  $C_L=120\mu F$ )



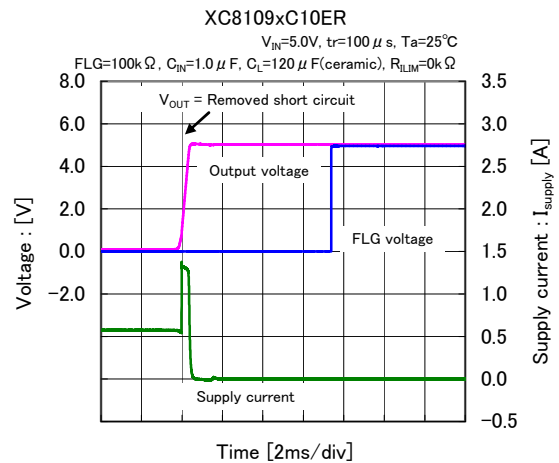
(30) Short-circuit transient response  
( $V_{OUT}$ =short $\rightarrow 5.0\Omega$ ,  $C_L=120\mu F$ )



(31) Short-circuit transient response  
( $V_{OUT}$ =open $\rightarrow$ short,  $C_L=120\mu F$ )

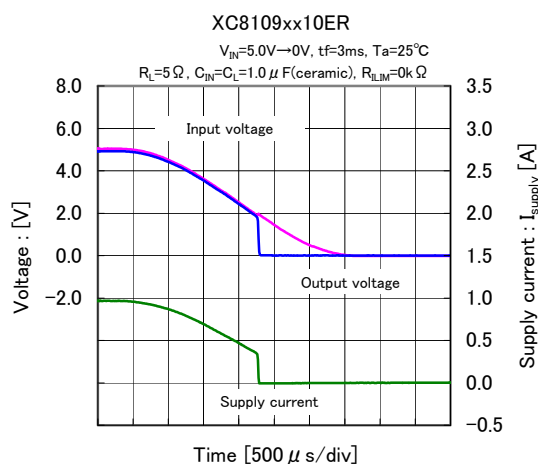
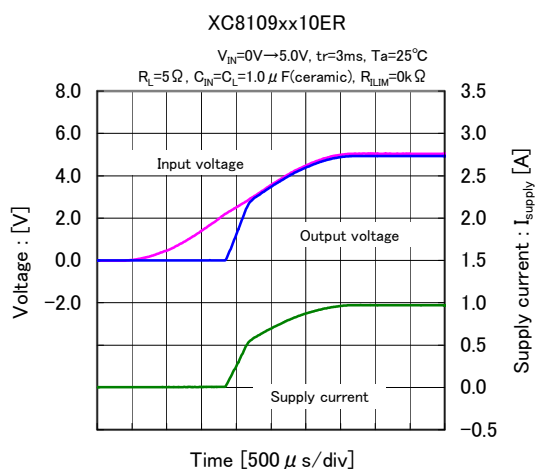


(32) Short-circuit transient response  
( $V_{OUT}$ =short $\rightarrow$ open,  $C_L=120\mu F$ )

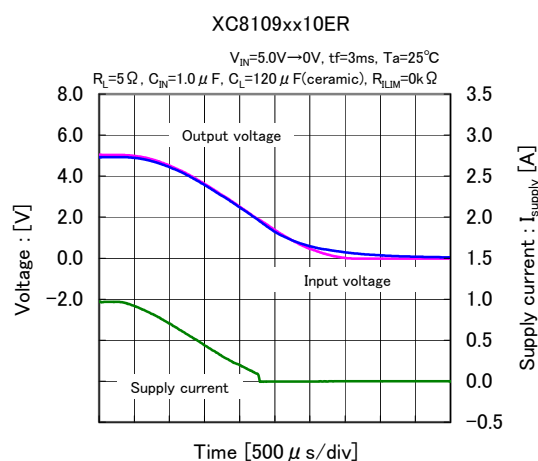
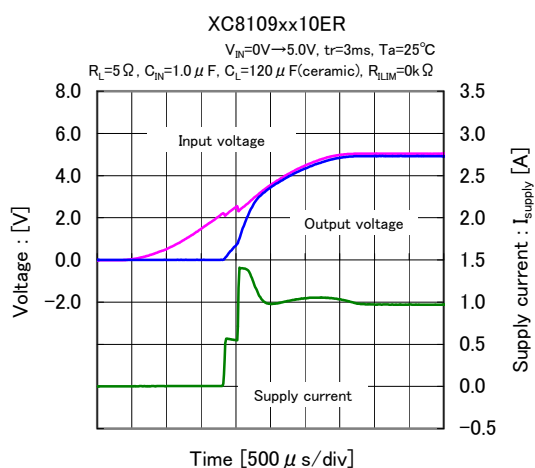


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

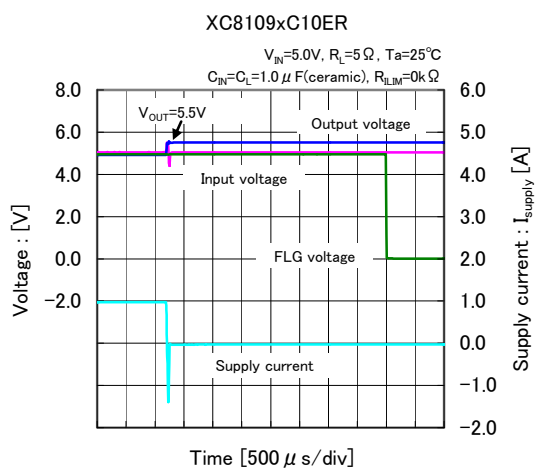
(33) UVLO transient response ( $C_L=1.0\ \mu\text{F}$ )



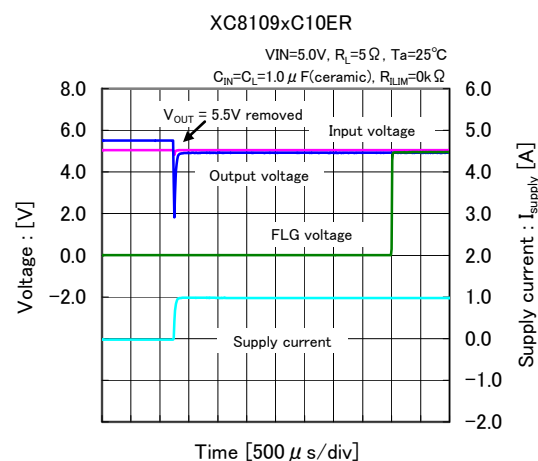
(34) UVLO transient response ( $C_L=120\ \mu\text{F}$ )



(35) Reverse voltage detected voltage ( $C_L=1.0\ \mu\text{F}$ )

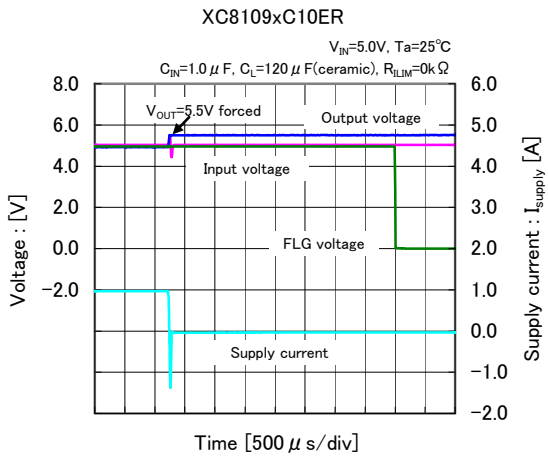


(36) Reverse voltage released voltage ( $C_L=1.0\ \mu\text{F}$ )

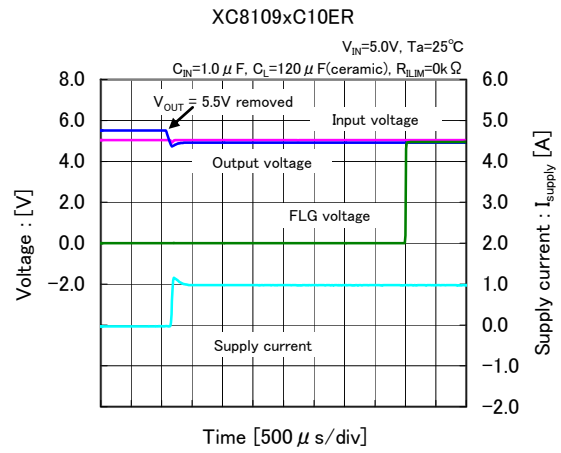


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

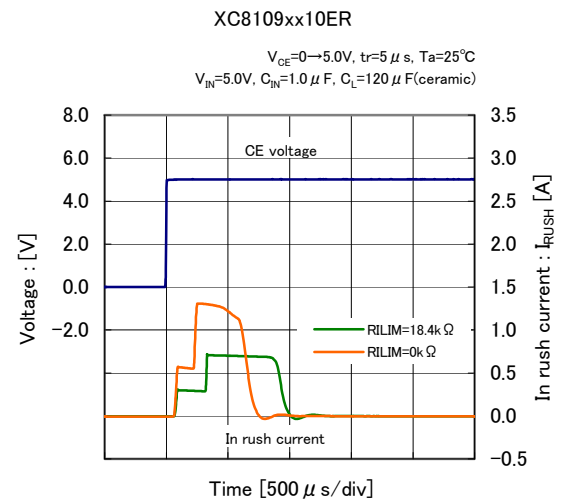
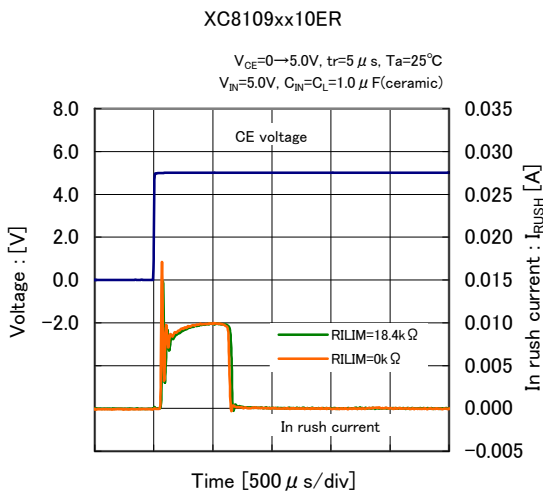
(37) Reverse voltage detected voltage ( $C_L=120\ \mu\text{F}$ )



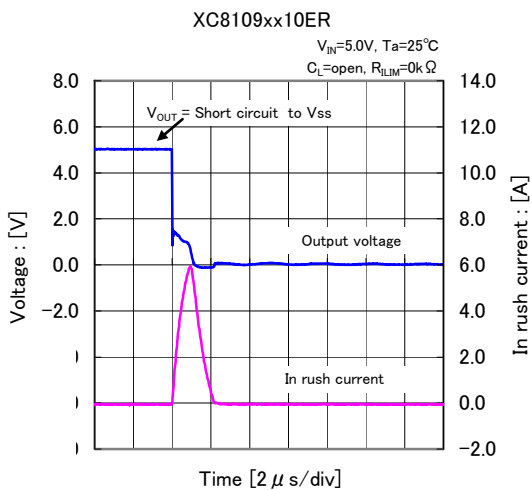
(38) Reverse voltage released voltage ( $C_L=120\ \mu\text{F}$ )



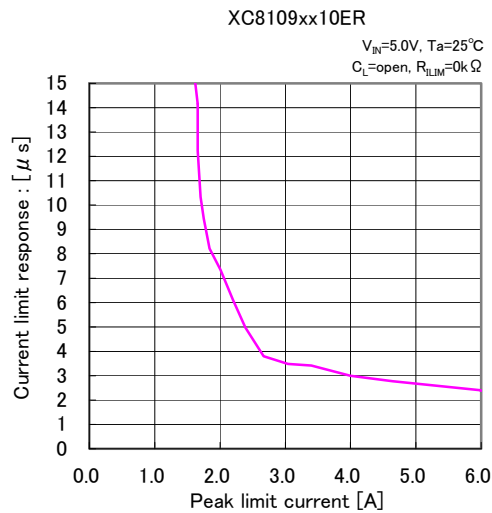
(39) CE transient response



(40) Short applied

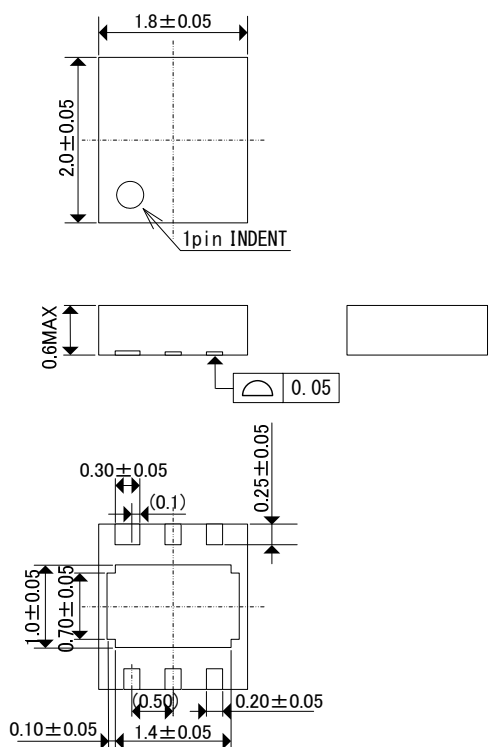


(41) Current limit adapted time

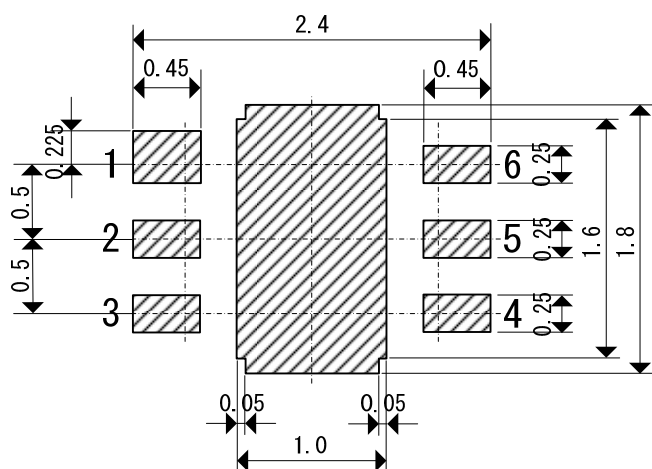


## PACKAGING INFORMATION

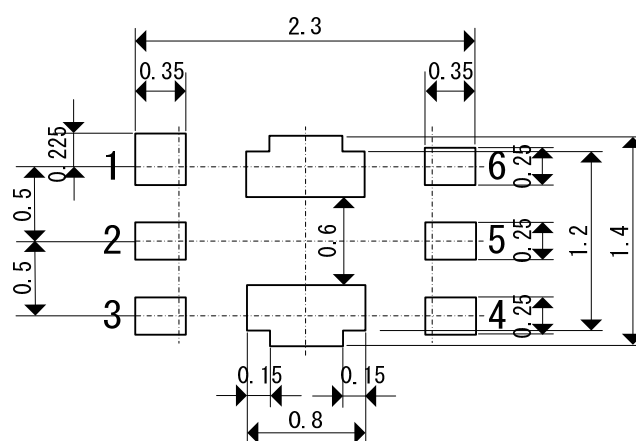
● USP-6C (unit:mm)



● USP-6C Reference Pattern Layout (unit: mm)



● USP-6C Reference Metal Mask Design (unit: mm)



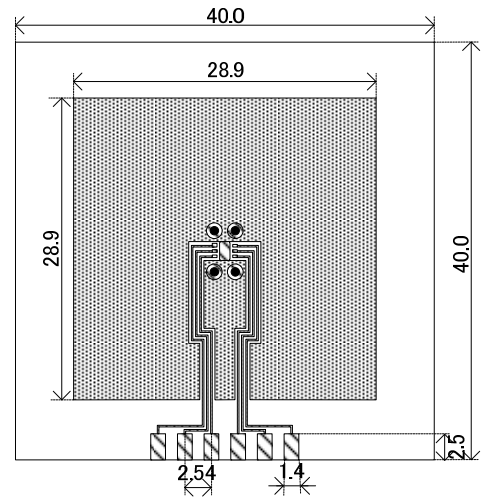
## PACKAGING INFORMATION (Continued)

### ● USP-6C Power Dissipation (40mm x 40mm Standard board)

Power dissipation data for the USP-6C is shown in this page.  
 The value of power dissipation varies with the mount board conditions.  
 Please use this data as the reference data taken in the following condition.

#### 1. Measurement Condition

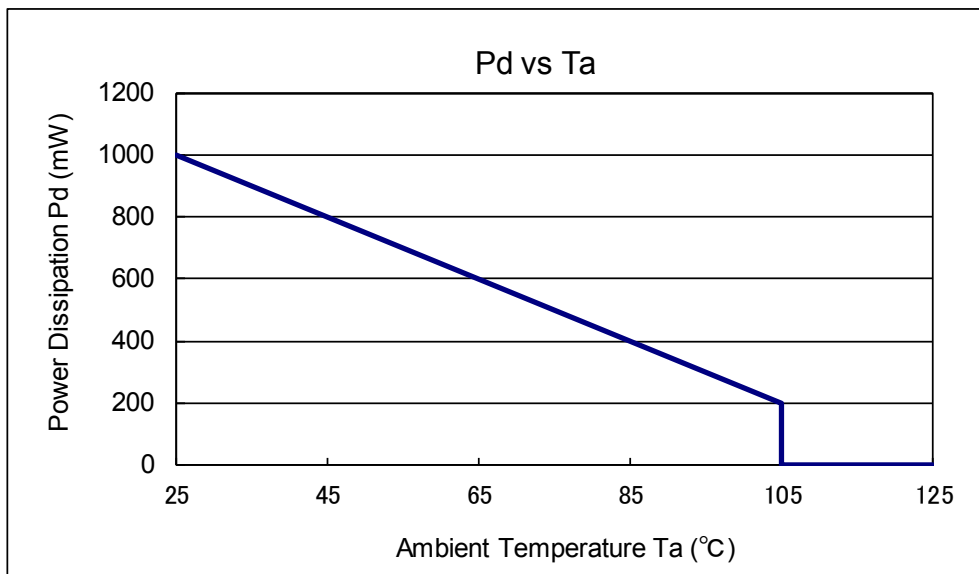
- Condition : Mount on a board
- Ambient : Natural convection
- Soldering : Lead (Pb) free
- Board : Dimensions 40 x 40 mm  
 (1600 mm<sup>2</sup> in one side)
- Copper (Cu) traces occupy 50% of the board  
 area in top and back faces
- Package heat-sink is tied to the copper traces
- Material : Glass Epoxy (FR-4)
- Thickness : 1.6mm
- Through-hole : 4 x 0.8 Diameter



#### 2. Power Dissipation vs. Ambient Temperature

Board Mount (T<sub>J</sub> max = 125°C)

Ambient Temperature (°C)	Power Dissipation Pd (mW)	Thermal Resistance (°C/W)
25	1000	100.00
105	200	





## ■ PACKAGING INFORMATION (Continued)

### ● USP-6C Power Dissipation (JEDEC board)

Power dissipation data for the USP-6C is shown in this page.

The value of power dissipation varies with the mount board conditions.

Please use this data as one of reference data taken in the described condition.

#### 1. Measurement Condition (Reference data)

Condition : Mount on a board

Ambient : Natural convection

Soldering : Lead (Pb) free

Board : The board using 4 copper layer.

(76.2mm×114.3mm - - Area: about 8700mm<sup>2</sup>)

1st layer : No copper foil (Signal layer)

2nd layer : 70mm×70mm\_Connected to heat-sink.

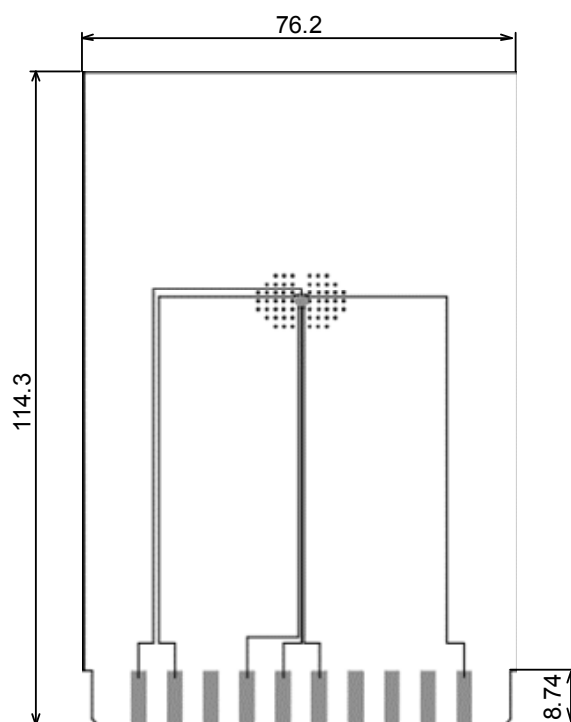
3rd layer : 70mm×70mm\_Connected to heat-sink.

4th layer : No copper foil (Signal layer)

Material : Glass Epoxy (FR-4)

Thickness : 1.6mm

Through-hole : φ0.2mm x 60pcs

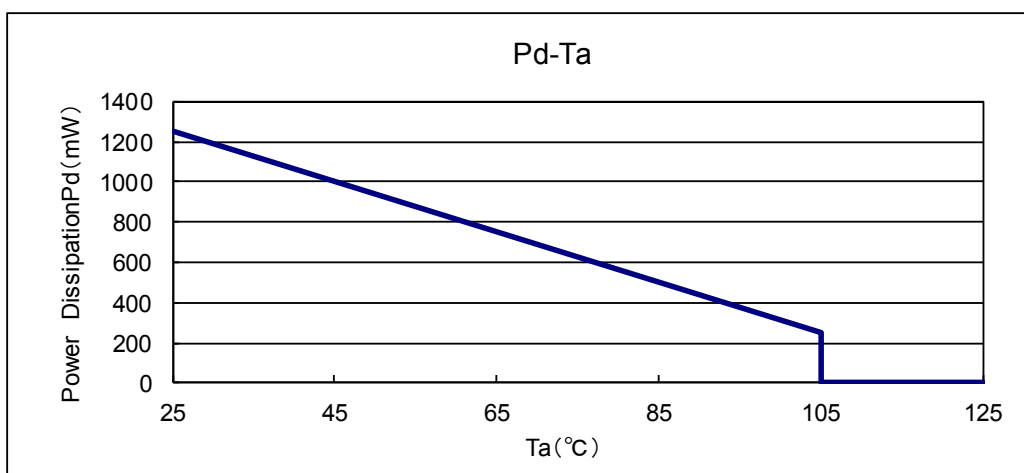


Evaluation Board (Unit: mm)

#### 2. Power Dissipation vs. Ambient temperature

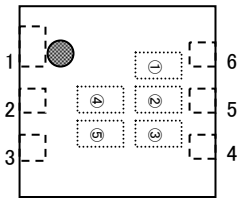
Board Mount(T<sub>jmax</sub> = 125°C)

Ambient Temperature (°C)	Power Dissipation Pd (mW)	$\theta_{ja}$ (°C/W)
25	1250	80.00
105	250	



## MARKING RULE

USP-6C



① represents products series

MARK	PRODUCT SERIES
Z	XC8109*****-G

② represents product type

MARK	CE LOGIC	PROTECTION CIRCUIT TYPE	PRODUCT
1	Active High	Auto-recovery	XC8109AC****-G
2	Active High	Latch-off	XC8109AD****-G
3	Active Low	Auto-recovery	XC8109BC****-G
4	Active Low	Latch-off	XC8109BD****-G

③ represents maximum output current

MARK	CURRENT (A)	PRODUCT SERIES
6	0.9	XC8109**10**-G

④⑤ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order.

(G, I, J, O, Q, W excluded)

\* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.
2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.
3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.
4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.
5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.
6. Our products are not designed to be Radiation-resistant.
7. Please use the product listed in this datasheet within the specified ranges.
8. We assume no responsibility for damage or loss due to abnormal use.
9. All rights reserved. No part of this datasheet may be copied or reproduced unless agreed by Torex Semiconductor Ltd in writing in advance.

TOREX SEMICONDUCTOR LTD.