TI Designs: TIDA-01247
Efficient, LDO-Less, Power Supply Network Reference Design for RF-Sampling ADC

Description

The power supply network design demonstrates a simplified and efficient network to power an ADC32RFxx. All three power domains of the analog-to-digital converter (ADC) are supplied using a switching regulator to enable the use of a power supply network without a low-dropout linear regulator (LDO). This configuration improves the overall power efficiency and reduces the part count without any degradation to the ADC specifications.

Resources

TIDA-01247	Design Folder
ADC32RF45	Product Folder
ADC32RF45EVM	Product Folder
TPS62085	Product Folder
TSW14J56EVM	Product Folder

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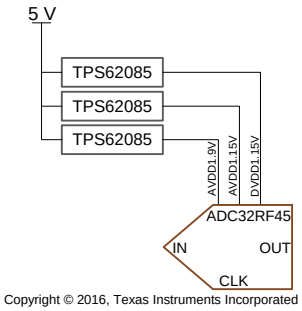
Features

- Power Savings of Approximately 900-mW With Dual-Channel Operation
- Power Efficiency Increased by More Than 10%
- Linear Regulators Not Required to Supply Clean Power to ADC
- Maintains ADC Performance Metrics
- Smaller DC-DC Solution Size and Fewer Components Than LDO-Based Design
- Supports Single 5-V Input

Applications

- Multi-Band, Multi-Mode (2G/3G/4G) Cellular Traffic and Feedback Receivers
- Software-Defined Radios
- Phased-Array Radars
- Cable Infrastructure
- High-Speed Digitizers, Communication Test Equipment



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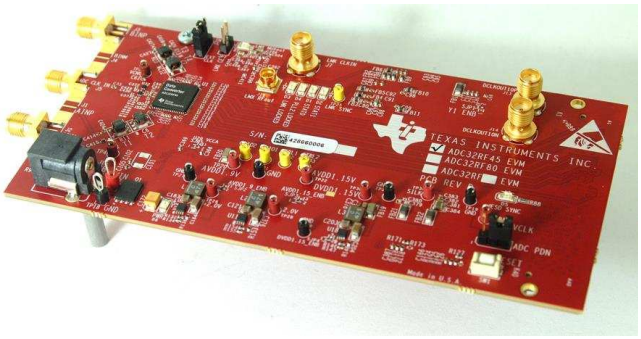

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1 System Description

ADC32RF45 is a dual-channel, 14-bit, 3-GSPS analog-to-digital converter (ADC) that supports RF sampling with input frequencies up to 4 GHz. Designed for high signal-to-noise ratio (SNR), the ADC delivers a noise spectral density of –155 dBFs/Hz. With the option to bypass digital down-conversion (DDC) and decimation, the full Nyquist bandwidth is available for digital processing to provide a high-performance and high-bandwidth ADC for the system designer. The device comes with only three power domains which simplify its power supply network design. The three power domains are: AVDD1.9V and AVDD1.15V for analog and DVDD1.15V for digital.

The product evaluation module (EVM) has a default option to power the analog domains with a low-noise low-dropout linear regulator (LDO) to minimize any impairments from the supply network. The purpose of this function is to extract the maximum performance and showcase the true capability of the device. This method may be optimal for performance, but it certainly is not the most cost-effective and efficient solution. A solution with a single supply input (5 V, for example) requires a switching regulator to step down the 5-V input to an intermediate level to prevent the LDO from a thermal shutdown. The use of a switching regulator increases the overall part count in addition to lowering efficiency. The issue of part count increases in multiple-input, multiple-output (MIMO) applications where many such devices can run synchronously. In such cases, the number of active devices is often limited due to issues with thermal management.

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2 System Overview

2.1 Block Diagram

This reference design presents a simplified power supply network for the ADC, where all three power domains are supplied from a DC-DC regulator (see Figure 1). This implementation improves the efficiency and reduces the part count in comparison to a solution using LDOs.

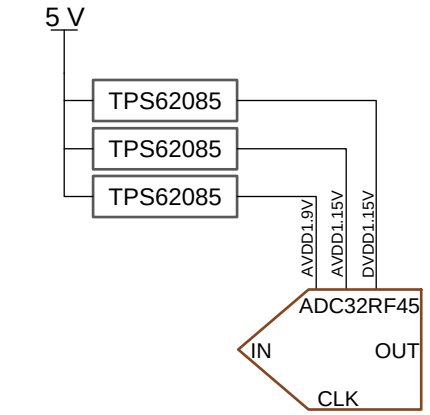

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Figure 1. TIDA-01247 Block Diagram

2.2 Design Considerations

If implementation with DC-DC converters is desired, be sure to check for noise and spurious contents that results from high current in the switching elements and the magnetics involved. Use careful layout techniques to reduce ground loop and bounce. The switching frequency spur in this design is filtered out using a ferrite bead. The high currents running in a switching power supply produce strong magnetic fields that can couple into other magnetic components on the board power, like transformers at the ADC analog and clock inputs. The designer can mitigate this conflict with careful floor planning and layout techniques.

The EVM offers a variety of decoupling capacitors to reduce ripple and provide filtering. This design retains most of the decoupling capacitors and only removes the redundant ones.

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2.3 Highlighted Products

2.3.1 ADC32RF45

The key device in this design is the ADC32RF45. The low noise floor and high bandwidth of the ADC enables it for use in a variety of diverse applications, including telecommunications and radar. The ADC32RF45 has a multi-band DDC block for each channel. This DDC block down-converts two separate frequency bands simultaneously for each channel or up to four bands for the entire device. The DDC block allows offloading of digital mixing and decimation from the field-programmable gate array (FPGA) in addition to reducing the total data throughput and power consumption of the interface. The flexibility to use a single down-converter per ADC channel allows the designer to switch the mixing frequency by switching between three independent, numerically-controlled oscillators (NCOs) per channel. Phase coherency is maintained by running the NCOs continuously, even when they have not been selected. The block diagram for the ADC32RF45 in Figure 2 shows the various DDCs as well as the DDC bypass, which can be used to enable the full data rate.

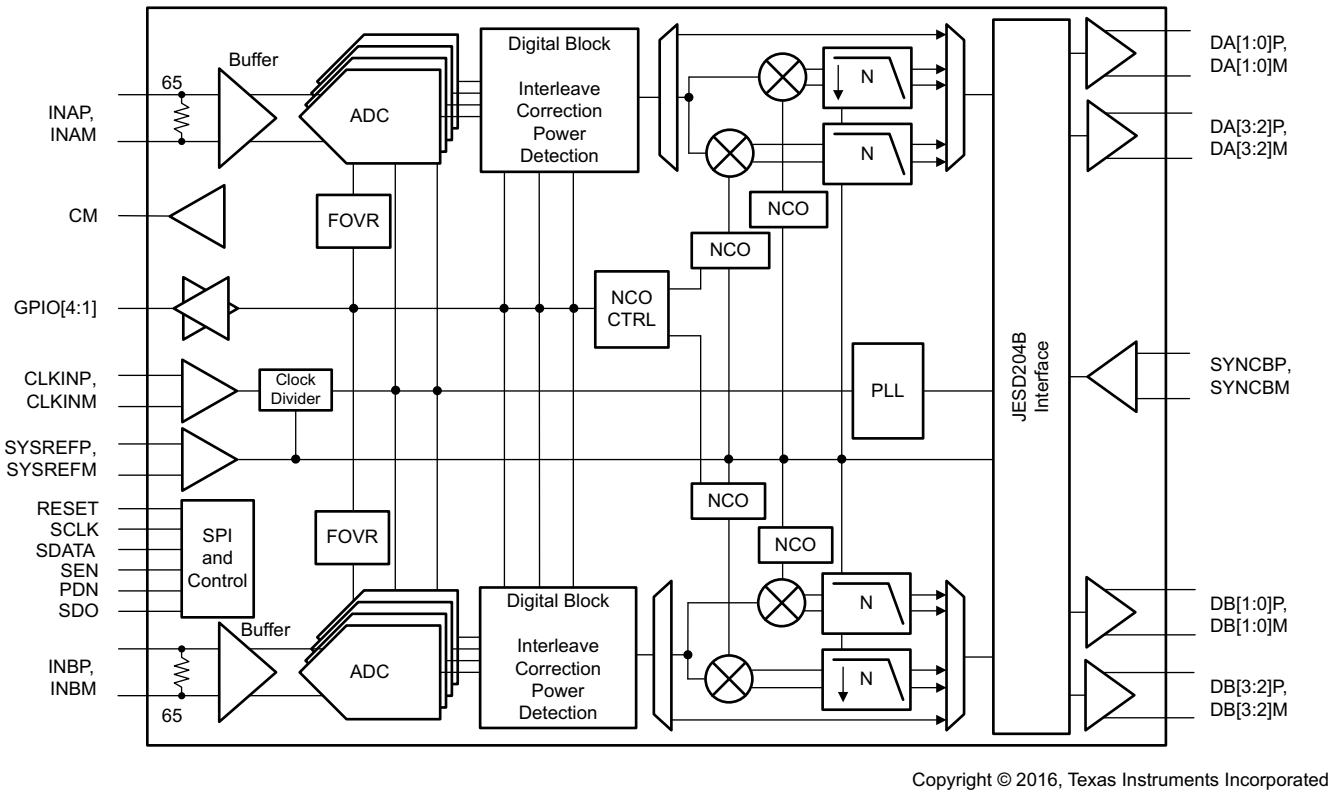

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Figure 2. ADC32RF45 Block Diagram

2.3.2 TPS62085

The TPS62085 device is a high-frequency, synchronous step-down converter optimized for small solution size and high efficiency. The device offers an input voltage range of 2.5 V to 6.0 V, which supports common battery technologies. The device focuses on a high-efficiency step-down conversion over a wide output current range. At medium-to-heavy loads, the converter operates in pulse-width modulation (PWM) mode and automatically enters power save mode operation at a light load to maintain high efficiency over the entire load current range. The internal compensation circuit allows a large selection of external output capacitor values ranging from 10 µF to 150 µF. The devices are available in a 2-mm × 2-mm QFN package.

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3 Getting Started Hardware

3.1 ADC32RF45 EVM

This design can be realized by using the ADC32RF45 EVM with some modifications. For more details, refer to the ADC32RF45 EVM tool folder: http://www.ti.com/tool/adc32rf45evm.

The modifications on the EVM to implement this design involve removing and modifying the values of a few components relevant to the AVDD1.9V and AVDD1.15V supply domains.

3.2 TSW14J56 EVM

For more details on the TSW14J56 EVM, refer to the TSW14J56 EVM tool folder: http://www.ti.com/tool/tsw14j56evm.

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4 Tests and Results

4.1 Test Methodology

Two power supply options are viable to assess the performance of the ADC in this design:

1. Option 1: The analog domains are powered by an LDO and the digital domains are powered with a switching regulator, as shown Figure 3 shows. This option is the default power supply network (PSN) in the EVM, which has been optimized for performance and is used as the benchmark.
2. Option 2 (TIDA-01247): All three power domains are supplied from switching regulators and form the basis of this reference design. Figure 4 and Figure 5, respectively, show the block diagram and modified network (on the ADC32RF45EVM) used to implement this option.

Performance of the ADC with these two options have been tested on the product EVM with minor modifications.

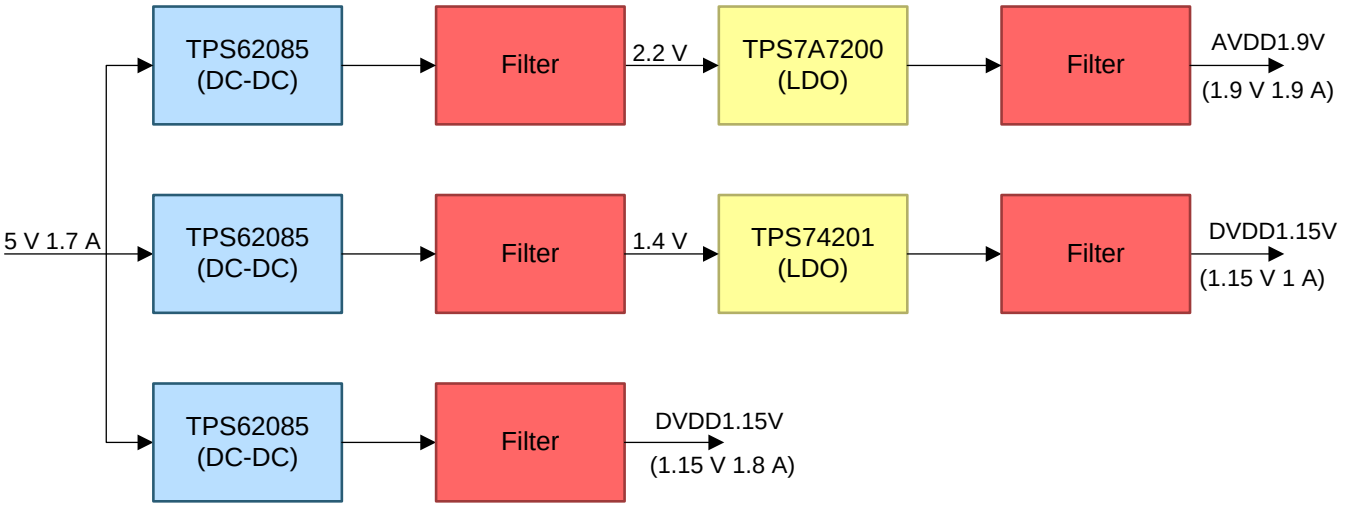

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Figure 3. PSN Option 1: Default PSN in EVM

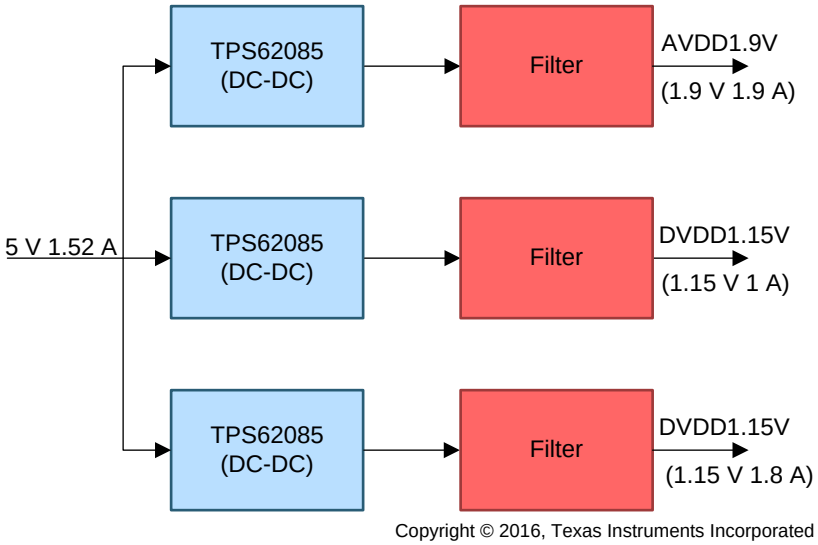

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Figure 4. PSN Option 2: Basis of TIDA-01247

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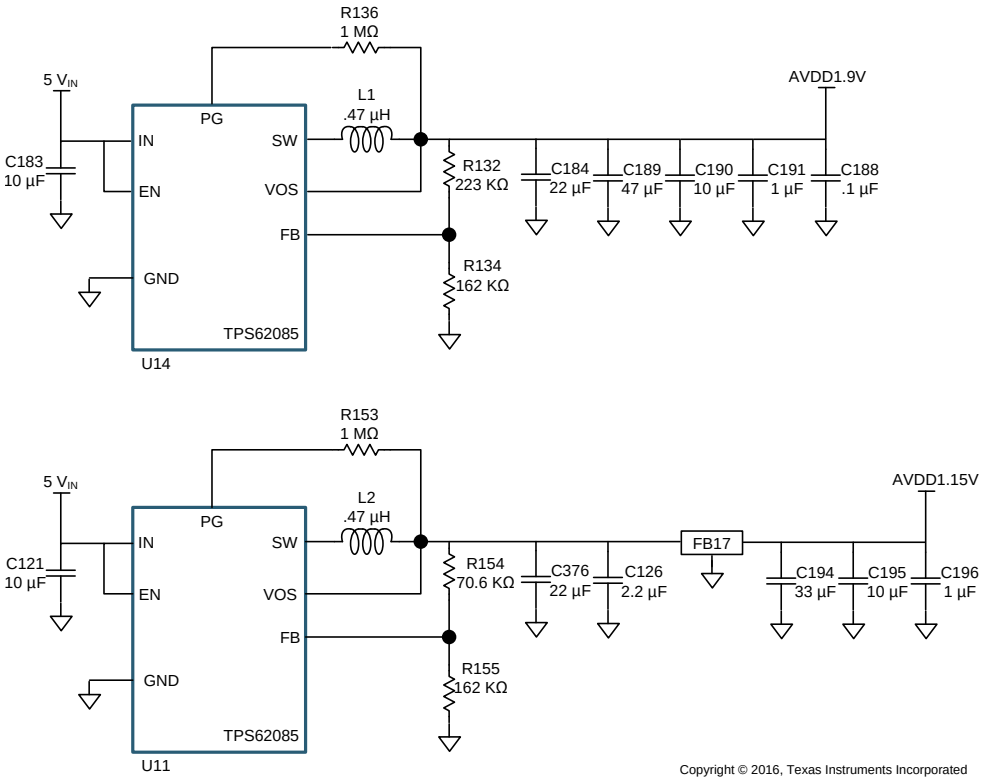

Figure 5. Modified AVDD1.9V and AVDD1.15V Supply Network to Implement TIDA-01247

4.2 Test Conditions

The two PSN options are tested under the same conditions. The ADC is operated at the maximum-supported sampling clock frequency of 3 GHz, which is derived from an external signal generator. The device is configured to bypass the digital decimation and down-conversion with the SerDes running at 12 Gbps. A single-tone CW at frequencies in popular telecommunication bands is used as input to channel B. The input power is set such that the fundamental amplitude at the digital output is –2 dBFs. Both RF and clock inputs are band-pass filtered for improved performance. The device register settings are set per the ADC32RF45 data sheet. Figure 6 shows the test setup.

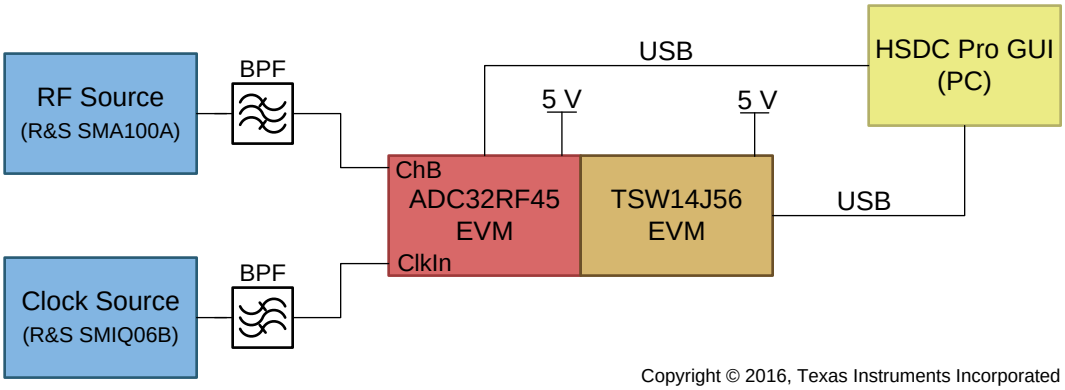

Figure 6. Test Setup for Evaluation of TIDA-01247

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4.3 Test Results

Table 1 and Table 2 show the SNR and SFDR performance, respectively, for the two power supply network options at different frequencies.

Table 1. SNR Performance Comparison (dBFs)

INPUT FREQUENCY	EVM DEFAULT (OPTION 1)	TIDA-01247 (OPTION #)
940M	60.6	60.8
1850M	57.3	57.4
2100M	56.5	55.9
2600M	55.1	55.2

Table 2. SFDR Performance Comparison (dBFs)

INPUT FREQUENCY	EVM DEFAULT (OPTION 1)	TIDA-01247 (OPTION 2)
940M	60.9	59.9
1850M	64.5	65.7
2100M	62.4	62.2
2600M	56.3	56.6

Figure 7 and Figure 8 show the fast-Fourier transform (FFT) plots for option 1 and option 2, respectively, at an input frequency of 1850 MHz. In this case, the fundamental in the second Nyquist is folded back and appears at 1150 MHz at the digital output. No significant difference in SNR is observable. Option 2 shows noticeable improvement in HD2 and HD3.

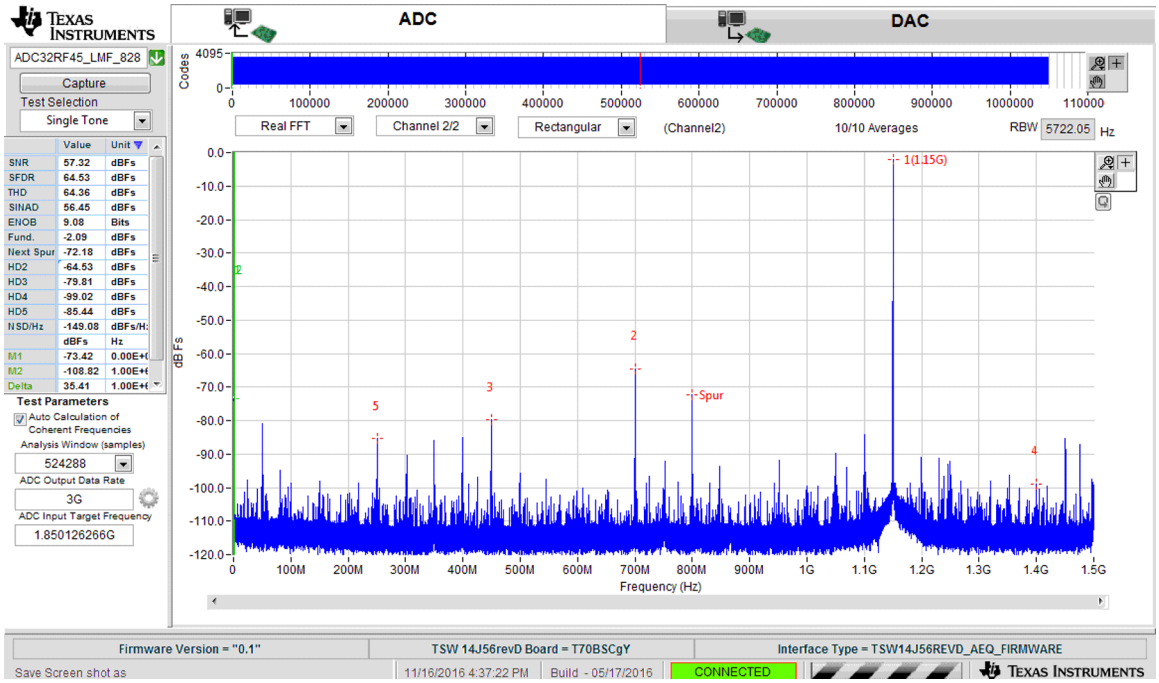

Figure 7. Single-Tone FFT at 1850-MHz Input With Option 1 (EVM Default)

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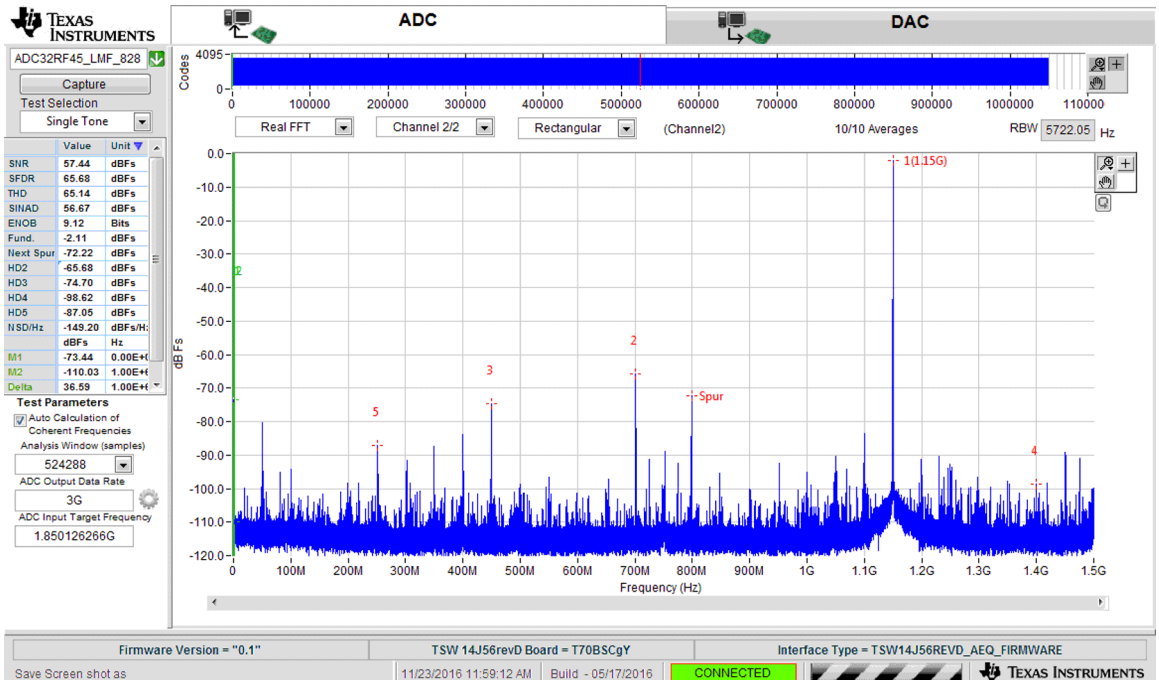

Figure 8. Single-Tone FFT at 1850-MHz Input With Option 1 (TIDA-01247)

Table 3 compares the current and power consumption for the two PSN options.

Table 3. Comparison of Current and Power Consumption

CONDITION	CURRENT	POWER
EVM default (option 1)	1.7 A	8.5 W
TIDA-01247 (option 2)	1.52 A	7.6 W
Savings	180 mA	900 mW

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5 Design Files

5.1 Schematics

To download the ADC32RF45 EVM schematics, see the design files at TIDA-01247. This design is based on the ADC32RF45 EVM with minor modifications as described in the preceding Figure 5.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01247. The BOM includes the modifications required on the ADC32RF45EVM.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01247.

5.4 Design Project

To download the Design project files, see the design files at TIDA-01247.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01247.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01247.

6 Software Files

To download the software files, see the design files at TIDA-01247.

7 Related Documentation

1. Texas Instruments, *ADC32RF45 Dual-Channel, 14-Bit, 3.0-GSPS, Analog-to-Digital Converter*, ADC32RF45 Data Sheet (SBAS747)
2. Texas Instruments, *ADC32RF45/RF80 EVM Quick Startup Guide*, ADC32RF45/RF80 EVM User's Guide (SLAU620)
3. Texas Instruments, *TPS6208x 3-A Step-Down Converter With Hiccup Short-Circuit Protection In 2 × 2 QFN Package*, TPS62085x Data Sheet (SLVSB70)

7.1 Trademarks

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8 About the Author

SATISH UPPATHIL is an applications engineer with the High Speed Products group. He received his bachelor's of technology in computer science from the University of Kerala-India and MSEE from the North Carolina State University in 2002 and has been working in the telecommunications and semiconductor industry since.

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