# PLL/Multibit Σ-Δ DAC

# AD1958



## FEATURES

- 5 V Stereo Audio DAC System
- Accepts 16-/18-/20-/24-Bit Data
- Supports 24 Bits, 192 kHz Sample Rate
- Accepts a Wide Range of Sample Rates Including: 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz
- Multibit Sigma-Delta Modulator with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DAC—Least Sensitive to Jitter
- Single-Ended Output for Easy Use
- 108 dB Signal-to-Noise (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
- 109 dB Dynamic Range (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
- –96 dB THD + N (Stereo)
- 75 dB Stop Band Attenuation
- On-Chip Clickless Volume Control
- Hardware and Software Controllable Clickless Mute
- Serial (SPI) Control for: Serial Mode, Number of Bits, Sample Rate, Volume, Mute, De-Emphasis
- Digital De-Emphasis Processing for 32 kHz, 44.1 kHz, and 48 kHz Sample Rates
- Programmable Dual Fractional-N PLL Clock Generator
- 27 MHz Master Clock Oscillator
- Better than 100 ps rms Master Clock Jitter
- Generated System Clocks
  - SCLK0: 33.8688 MHz
  - SCLK1: 22.5792 MHz, 24.576 MHz, 33.8688 MHz, or 36.864 MHz
  - SCLK2: 16.9344 MHz
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible, and DSP Serial Port Modes
- 28-Lead SSOP Plastic Package

## APPLICATIONS

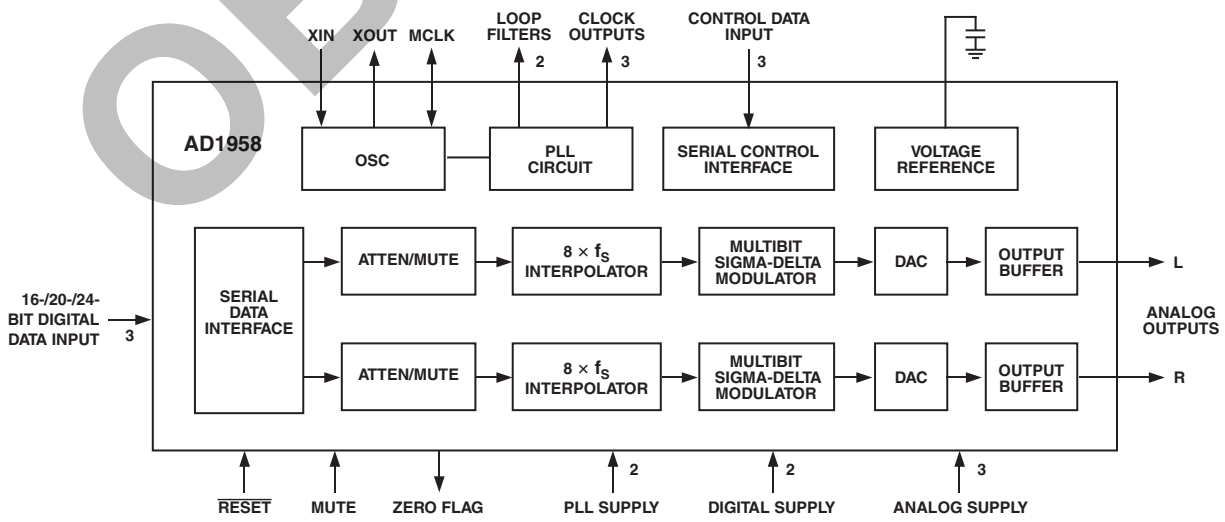
DVD, CD, Home Theater Systems, Automotive Audio Systems, Sampling Musical Keyboards, Digital Mixing Consoles, Digital Audio Effects Processors

## PRODUCT OVERVIEW

The AD1958 is a complete high-performance single-chip stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator, digital interpolation filters, and analog output drive circuitry with an on-board dual PLL clock generator. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port. The AD1958 is fully compatible with all known DVD formats including 96 kHz and 192 kHz sample frequencies and 24 bits. It also is backwards-compatible by supporting 50 µs/15 µs digital de-emphasis for "redbook" compact discs, as well as de-emphasis at 32 kHz and 48 kHz sample rates.

The AD1958 has a simple but flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers, and sample rate converters. The AD1958 can be configured in left-justified, I²S, right-justified, or DSP serial-port-compatible modes. It can support 16, 20, and 24 bits in all modes. The AD1958 accepts serial audio data in MSB first, two's-complement format, and operates from a single 5 V power supply. It is fabricated on a single monolithic integrated circuit and housed in a 28-lead SSOP package for operation over the temperature range –40°C to +105°C.

## FUNCTIONAL BLOCK DIAGRAM




REV. 0



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# AD1958–SPECIFICATIONS

**TEST CONDITIONS UNLESS OTHERWISE NOTED**

| | |
|---|---|
| Supply Voltages | |
| (AVDD, DVDD, PVDD) | 5.0 V |
| Ambient Temperature | 25°C |
| Input Clock | 12.288 MHz (256 × $f_S$ Mode) |
| Input Signal | 996.0938 Hz, 0 dB Full Scale |
| Input Sample Rate | 48 kHz |
| Measurement Bandwidth | 20 Hz to 20 kHz |
| Word Width | 24 Bits |
| Load Capacitance | 100 pF |
| Load Impedance | 47 kΩ |
| Input Voltage HI | 2.0 V |
| Input Voltage LO | 0.8 V |

**ANALOG PERFORMANCE**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Resolution | | 24 | | Bits |
| Signal-to-Noise Ratio (20 Hz to 20 kHz) | | | | |
| No Filter (Stereo) | | 105 | | dB |
| With A-Weighted Filter (Stereo) | | 108 | | dB |
| Dynamic Range (20 Hz to 20 kHz, –60 dB Input) | | | | |
| No Filter (Stereo) | | 105 | | dB |
| With A-Weighted Filter (Stereo) | 102 | 109 | | dB |
| Total Harmonic Distortion + Noise (Stereo) | –90 | –96 | | dB |
| PLL Performance | | | | |
| Master Clock Input Frequency | | 27 | | MHz |
| Generated System Clocks | | | | |
| SCLK0 | | 33.8688 | | MHz |
| SCLK1 | | 12.288 | | MHz |
| SCLK2 | | 22.5792 | | MHz |
| Jitter (SCLK0 and SCLK1) | | 110 | 175 | ps rms |
| Jitter (MCLK) | | 60 | 100 | ps rms |
| Duty Cycle (SCLK0, SCLK1)[1] | | 50 | | % |
| Duty Cycle (MCLK) | 49 | 50 | 51 | % |
| Analog Outputs | | | | |
| Single-Ended Output Range (±Full Scale) | | 3.17 | | V p-p |
| Output Capacitance at Each Output Pin | | | 2 | pF |
| Out-of-Band Energy (0.5 × $f_S$ to 100 kHz) | | | –90 | dB |
| $V_{REF}$ (FILTR) | | 2.39 | | V |
| DC Accuracy | | | | |
| Gain Error | –5 | ±2.0 | +5 | % |
| Interchannel Gain Mismatch | –0.15 | ±0.015 | +0.15 | dB |
| Gain Drift | | 150 | 250 | ppm/°C |
| DC Offset | –25 | –3 | +20 | mV |
| Interchannel Crosstalk (EIAJ Method) | | –120 | | dB |
| Interchannel Phase Deviation | | ±0.1 | | Degrees |
| Mute Attenuation | | –100 | | dB |
| De-Emphasis Gain Error | | | ±0.1 | dB |

NOTES

[1]In some combinations with Clock Configuration Mode = 1 (see Table III), SCLK will not be 50%.

[2]Performance of right and left channels is identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).

Specifications subject to change without notice.

**DIGITAL I/O** (–40°C to +105°C )

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input Voltage HI ($V_{IH}$) | 2.0 | | | V |
| Input Voltage LO ($V_{IL}$) | | | 0.8 | V |
| Input Leakage ($I_{IH}$ @ $V_{IH}$ = 2.4 V) | | | 10 | µA |
| Input Leakage ($I_{IL}$ @ $V_{IL}$ = 0.8 V) | | | 10 | µA |
| High Level Output Voltage ($V_{OH}$) $I_{OH}$ = 1 mA | 3.5 | | | V |
| Low Level Output Voltage ($V_{OL}$) $I_{OL}$ = 1 mA | | | 0.4 | V |
| Input Capacitance | | | 20 | pF |

Specifications subject to change without notice.

**TEMPERATURE RANGE**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Specifications Guaranteed | | 25 | | °C |
| Functionality Guaranteed | –40 | | +105* | °C |
| Storage | –55 | | +125 | °C |

NOTE
*105°C ambient guaranteed for a 4-layer board, two 1 oz. planes, two 2 oz. signal layers. Derate to 85°C for 2-layer board, 2 oz. layers.

Specifications subject to change without notice.

**POWER**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supplies | | | | |
| Voltage, Analog Digital PLL | 4.50 | 5 | 5.50 | V |
| Analog Current | | 36 | 41 | mA |
| Digital Current | | 25 | 29 | mA |
| PLL Current | | 30 | 34 | mA |
| Dissipation | | | | |
| Operation—All Supplies | | 455 | 540 | mW |
| Operation—Analog Supply | | 180 | | mW |
| Operation—Digital Supply | | 125 | | mW |
| Operation—PLL Supply | | 150 | | mW |
| Power Supply Rejection Ratio | | | | |
| 1 kHz 300 mV p-p Signal at Analog Supply Pins | | –60 | | dB |
| 20 kHz 300 mV p-p Signal at Analog Supply Pins | | –50 | | dB |

Specifications subject to change without notice.

**DIGITAL FILTER CHARACTERISTICS**

| Sample Rate (kHz) | Pass Band (kHz) | Stop Band (kHz) | Stop Band Attenuation (dB) | Pass Band Ripple (dB) |
|---|---|---|---|---|
| 44.1 | DC–20 | 24.1–328.7 | 75 | ±0.0002 |
| 48 | DC–21.8 | 26.23–358.28 | 75 | ±0.0002 |
| 96 | DC–39.95 | 56.9–327.65 | 75 | ±0.0005 |
| 192 | DC–87.2 | 117–327.65 | 60 | 0/–0.04 (DC–21.8 kHz)<br>0/–0.5 (DC–65.4 kHz)<br>0/–1.5 (DC–87.2 kHz) |

Specifications subject to change without notice.

**GROUP DELAY**

| Chip Mode | Group Delay Calculation | $f_S$ | Group Delay | Unit |
|---|---|---|---|---|
| INT8× Mode | $24.625/f_S$ | 48 kHz | 513 | µs |
| INT4× Mode | $15.75/f_S$ | 96 kHz | 164 | µs |
| INT2× Mode | $14/f_S$ | 192 kHz | 72.91 | µs |

Specifications subject to change without notice.

**DIGITAL TIMING (Guaranteed over –40°C to +105°C, AVDD = DVDD = PVDD = 5.0 V ± 10%)**

| | | Min | Unit |
|---|---|---|---|
| $t_{DMP}$ | MCLK Period (FMCLK = 256 × FLRCLK) | 54 | ns |
| $t_{DML}$ | MCLK LO Pulsewidth (All Modes) | 15 | ns |
| $t_{DMH}$ | MCLK HI Pulsewidth (All Modes) | 10 | ns |
| $t_{DBH}$ | BCLK HI Pulsewidth | 20 | ns |
| $t_{DBL}$ | BCLK LO Pulsewidth | 20 | ns |
| $t_{DBP}$ | BCLK Period | 60 | ns |
| $t_{DLS}$ | LRCLK Setup | 20 | ns |
| $t_{DLH}$ | LRCLK Hold (DSP Serial Port Mode Only) | 20 | ns |
| $t_{DDS}$ | SDATA Setup | 15 | ns |
| $t_{DDH}$ | SDATA Hold | 15 | ns |
| $t_{RSTL}$ | RST LO Pulsewidth | 15 | ns |

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS***

DVDD to DGND . . . . . –0.3 V to +6 V
AVDD to DGND . . . . . –0.3 V to +6 V
Digital Inputs . . . . . DGND – 0.3 V to DVDD + 0.3 V
Analog Inputs . . . . . AGND – 0.3 V to AVDD + 0.3 V
AGND to DGND . . . . . –0.3 V to + 0.3 V
Reference Voltage . . . . . (AVDD + 0.3)/2
Soldering (10 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

**PACKAGE CHARACTERISTICS**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ (Thermal Resistance) Junction-to-Ambient (2-Layer Board) | | 109.0 | | °C/W |
| $\theta_{JA}$ (Thermal Resistance) Junction-to-Ambient (4-Layer Board— 2 Signal, 2 Planes) | | 78.58 | | °C/W |
| $\theta_{JA}$ (Thermal Resistance) Junction-to-Case | | 39.0 | | °C/W |

**CAUTION**

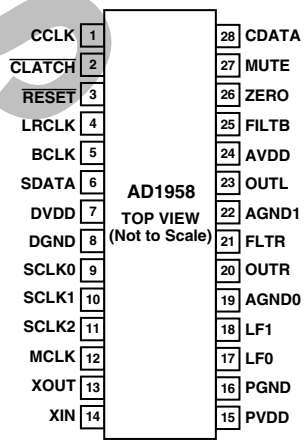
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1958 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.




**ORDERING GUIDE**

| Model | Temperature | Package Description | Package Option |
|---|---|---|---|
| AD1958YRS | –40°C to +105 °C | 28-Lead Small Outline Package | RS-28 |
| AD1958YRSRL | –40°C to +105 °C | 28-Lead Small Outline Package | RS-28 on 13" Reels |
| EVAL-AD1958EB | | Evaluation Board | |

**PIN CONFIGURATION**



**PIN FUNCTION DESCRIPTIONS**

| Pin | Input/Output | Mnemonic | Description |
|---|---|---|---|
| 1 | I | CCLK | Control Clock Input for Control Data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuous or gated. |
| 2 | I | $\overline{\text{CLATCH}}$ | Latch Input for Control Data |
| 3 | I | $\overline{\text{RESET}}$ | Reset. The AD1958 is placed in a reset mode when this pin is held LO. The serial control port registers are reset to their default values. Set HI for normal operation. |
| 4 | I | LRCLK | Left/Right Clock Input for Input Data. Must run continuously. |
| 5 | I | BCLK | Bit Clock Input for Input Data. Need not run continuously; may be gated or used in a burst fashion. |
| 6 | I | SDATA | Serial input, MSB first, containing two channels of 16/20/24 bits of two's-complement data per channel. |
| 7 | I | DVDD | Digital Power Supply Connect to Digital 5 V Supply |
| 8 | I | DGND | Digital Ground |
| 9 | O | SCLK0 | 33.8688 MHz Clock Output |
| 10 | O | SCLK1 | 256/384/512/768 $f_S$ Output |
| 11 | O | SCLK2 | 16.9344 MHz/22.5792 MHz/512 $f_S$ Output |
| 12 | I/O | MCLK | 27 MHz Master Clock Output/256 $f_S$ DAC Clock Input |
| 13 | O | XOUT | 27 MHz Crystal Oscillator Output |
| 14 | I | XIN | 27 MHz Crystal Oscillator/External Clock Input |
| 15 | | PVDD | PLL Power Supply. Connect to PLL 5 V Supply. |
| 16 | | PGND | PLL Ground |
| 17 | | LF0 | PLL0 Loop Filter |
| 18 | | LF1 | PLL1 Loop Filter |
| 19 | | AGND0 | Analog Ground |
| 20 | O | OUTR | Right Channel Positive Line Level Analog Output |
| 21 | O | FILTR | Voltage Reference Filter Capacitor Connection. Bypass and decouple the voltage reference with parallel 10 µF and 0.1 µF capacitors to AGND. |
| 22 | I | AGND1 | Analog Ground |
| 23 | O | OUTL | Left Channel Line Level Analog Output |
| 24 | | AVDD | Analog Power Supply. Connect to Analog 5 V Supply. |
| 25 | | FILTB | Filter Capacitor Connection. Connect 10 µF Capacitor to AGND. |
| 26 | O | ZERO | Zero Flag Output. This pin goes HI when both channels have zero signal input for more than 1024 L/R Clock Cycles. |
| 27 | I | MUTE | Mute. Assert HI to Mute Both Stereo Analog Outputs. Deassert LO for normal operation. |
| 28 | I | CDATA | Serial Control Input, MSB first, containing 16 bits of unsigned data per channel. Used for specifying channel-specific attenuation and mute. |



## FUNCTIONAL DESCRIPTION

### DAC

The AD1958 has two DAC channels arranged as a stereo pair with single-ended analog outputs. Each channel has its own independently programmable attenuator, adjustable in 16384 linear steps. Digital inputs are supplied through a serial data input pin, SDATA, a frame clock, LRCLK, and a bit clock, BLCK.

Each analog output pin sits at a dc level of $V_{REF}$ (present at FILTR), and swings ±1.585 V for a 0 dB digital input signal. A single op amp third-order external low-pass filter is recommended to remove high-frequency noise present on the output pins. The output phase can be changed in an SPI control register to accommodate inverting and noninverting filters. Note that the use of op amps with low slew rate or low bandwidth may cause high frequency noise and tones to fold down into the audio band; care should be exercised in selecting these components.

The FILTB and FILTR pins should be bypassed by external capacitors to ground. The FILTB pin is used to reduce the noise of the internal DAC bias circuitry, thereby reducing the DAC output noise. The voltage at the $V_{REF}$ pin, FILTR ($V_{REF}$ ~ 2.39 V) can be used to bias external op amps used to filter the output signals.

The DAC master clock frequency is 256 $f_S$ for the 32 kHz–48 kHz range (8× interpolation, see Table I). For the 96 kHz range (4× interpolation) this is 128 $f_S$. At 192 kHz (2× interpolation), this is 64 $f_S$. It is supplied internally from the PLL clock system when MCLK mode is set to Output in the PLL Control Register. When the MCLK mode is changed to Input, it must be supplied from an external source connected to MCLK. The output from the 27 MHz PLL clock is disabled in this case.

**Table I. DAC Control Register**

| Bit 11:10 | Bit 9:8 | Bit 7 | Bit 6 | Bit 5:4 | Bit 3:2 | Bit 1:0 |
|---|---|---|---|---|---|---|
| Interpolation Factor | Serial Data Width | Output Phase | Soft Mute | Serial Data Format | De-Emphasis Filter | SPI Register Address |
| 00 = 8×*<br>01 = 4×<br>10 = 2×<br>11 = Not Allowed | 00 = 24 Bits*<br>01 = 20 Bits<br>10 = 16 Bits<br>11 = 16 Bits | 0 = Noninverted*<br>1 = Inverted | 0 = No Mute*<br>1 = Muted | 00 = I²S*<br>00 = Right Justified<br>10 = DSP<br>11 = Left Justified | 00 = None*<br>01 = 44.1 kHz<br>10 = 32 kHz<br>11 = 48 kHz | 01 |

*Default Setting

## PLL CLOCK SYSTEM

The PLL clock system is expected to be run from a 27 MHz master clock supplied by the on-board crystal oscillator or an external source connected to XIN. With the MCLK mode set to Output, the 27 MHz clock is buffered out to the MCLK pin. When set to Input, this pin is the 256 $f_S$ master clock input for the DAC. SCLK0 is always set to 33.8688 MHz. SCLK1 is intended to be used as a master audio clock and will be a multiple of the sample rate set in the PLL control register (see Table III). In Mode 0 (Bit 8), it can be set to 512 or 768 times either 44.1 kHz or 48 kHz. SCLK2 will be 16.3944 MHz (384 × 44.1 kHz). In Mode 1, SCLK1 can be set to 256, 384, 512, or 768 times 32 kHz, 44.1 kHz, or 48 kHz. SCLK2 can be set to a constant 22.5792 MHz (512 × 44.1 kHz) or 512 $f_S$.

There are two loop filter pins, LF0 and LF1. They should each be bypassed to PVDD by a network consisting of a 33 nF capacitor in series with a 750 Ω resistor, paralleled with a 1.8 nF capacitor.

The 27 MHz Master Clock oscillator should have a crystal cut for an 18 pF load connected between XIN and XOUT, with 22 pF capacitors connected from XIN and XOUT to PGND.

**Table II. DAC Volume Registers**

| Bit 15:2 | Bit 1:0 |
|---|---|
| Volume | SPI Register Address |
| 14 Bits, Unsigned<br>14 Bits, Unsigned | 00 = Left Volume<br>10 = Right Volume |

Default is full volume

## RESET/POWER-DOWN

$\overline{\text{RESET}}$ will set the control registers to their default settings. The chip should be reset on power-up. After reset is deasserted, the part will come out of reset on the next rising LRCLK.

## SERIAL CONTROL PORT

The AD1958 has an SPI-compatible control port to permit programming the internal control registers for the PLL and DAC. The DAC output levels may be independently programmed by means of an internal digital attenuator adjustable in 16384 linear steps.

**Table III. PLL Control Register**

| Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7:6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1:0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL2 Power-Down | PLL1 Power-Down | XTAL Power-Down | Clock Configuration | $f_S$ | SCLK1 Select | Frequency Double[2] | SCLK2 Select | MCLK Mode | SPI Register Address |
| 0 = On[1]<br>1 = PD | 0 = On[1]<br>1 = PD | 0 = On[1]<br>1 = PD | 0 = Mode 0[1] | SCLK1 =<br>000: 36.864 MHz[1]<br>100: 24.576 MHz<br>110: 33.8688 MHz<br>111: 22.5792 MHz<br>Other combinations reserved<br>SCLK2 = 16.9344 MHz | | Reserved<br>Set to 0 | Reserved<br>Set to 0 | 0 = Output[1]<br>1 = Input | 11 |
| | | | 1 = Mode 1 | 00 = 48 kHz<br>01 = Not Allowed<br>10 = 32 kHz<br>11 = 44.1 kHz | 0 = 256 $f_S$<br>1 = 384 $f_S$ | 0 = Normal<br>1 = $f_{NOMINAL} \times 2$ | 0 = 22.5792 MHz<br>1 = 512 × $f_S$[2] | | |

NOTES
[1]Default Setting
[2]In Mode 1, Frequency Double affects SCLK1 always and SCLK2 in 512 × $f_S$ mode.

The SPI control port is a 3-wire serial control port. The format is similar to the Motorola SPI format except the input data word is 16 bits wide. Max serial bit clock frequency is 8 MHz and may be completely asynchronous to the PLL system or the DAC. Figure 1 shows the format of the SPI signal. Note that the CCLK can be gated or continuous, $\overline{\text{CLATCH}}$ should be low during the 16 active clocks.

**POWER SUPPLY AND VOLTAGE REFERENCE**

The AD1958 is designed for five-volt supplies. Separate power supply pins are provided for the analog, digital, and PLL sections. These pins should be bypassed with 100 nF ceramic chip capacitors, as close to the pins as possible, to minimize noise. A bulk aluminum electrolytic capacitor of at least 22 µF should also be provided on the same PC board. For best performance it is recommended that the analog supply be separate from the digital and PLL supply. It is recommended that all supplies be isolated by ferrite beads in series with each supply. It is expected that the digital and PLL sections will be run from a common supply but isolated from one another. It is important that the analog supply be as clean as possible.

The internal voltage reference is brought out on Pin 21 (FILTR) and should be bypassed as close as possible to the chip with a parallel combination of 10 µF and 100 nF. The reference voltage may be used to bias external op amps to the common-mode voltage of the analog output signal pins. The current drawn from the FILTR pin should be limited to less than 50 µA.

**SERIAL DATA PORTS—DATA FORMAT**

The DAC serial data input mode defaults to $I^2S$. By changing Bits 4 and 5 in the DAC control register, the mode can be changed to RJ, DSP, or LJ. The word width defaults to 24 bits but can be changed by programming Bits 8 and 9 in the DAC Control Register.

Figure 2 shows the serial mode formats.

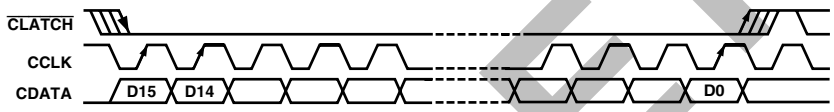
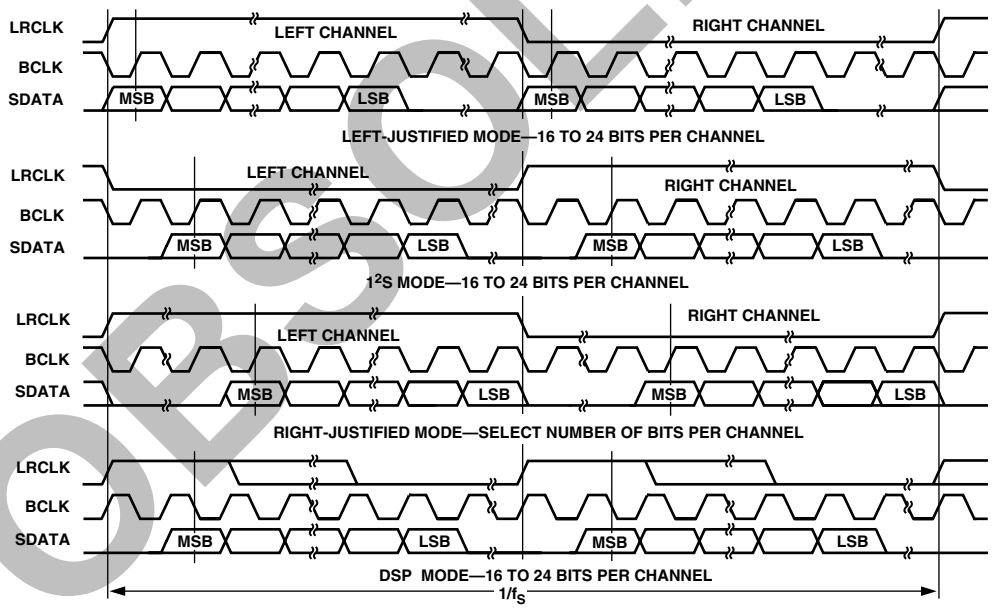



*Figure 1. Format of SPI Signal*



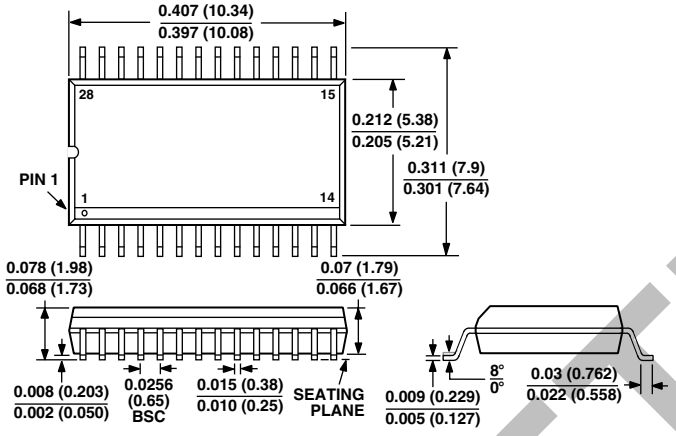

NOTES
1. DSP MODE DOES NOT IDENTIFY CHANNEL.
2. LRCLK NORMALLY OPERATES AT $f_S$ EXCEPT FOR DSP MODE WHICH IS 2 × $f_S$.
3. BCLK FREQUENCY IS NORMALLY 64 × LRCLK BUT MAY BE OPERATED IN BURST MODE.

*Figure 2. Stereo Serial Modes*

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 28-Lead Small Outline Package (SSOP)
### (RS-28)




CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN



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