Advanced Synchronous Rectifier Controller for LLC Resonant Converter

NCP4318

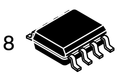
NCP4318 is an advanced synchronous rectification (SR) controller for LLC resonant converter with minimum external components. It has two gate drivers for driving the SR MOSFETs rectifying the outputs of the secondary transformer windings. The two gate drivers have their own drain and source sensing pins and operate independently of each other. The advanced adaptive dead time control compensates the voltage across parasitic inductance to minimize the body diode conduction and maximize the system efficiency. The advanced turn−off control algorithm allows stable SR operation over entire load range. NCP4318 has two versions of pin assignment – NCP4318A, NCP4318B, and two types of package – SOIC−8 and SOIC−8 EP.

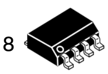
Features

- Mixed Mode SR Turn−off Control
- Anti Shoot−through Control for Reliable SR Operation
- 200 V−rated Drain Sensing and Dedicated Source Sensing Pins
- Advanced Adaptive Dead Time Control
- SR Current Inversion Detection
- Adaptive Minimum Turn−on Time for Noise Immunity
- SR Conduction Time Increase Rate Limitation
- Multi−level Turn−off Threshold Voltage
- Adaptive Gate Voltage (10 V, 6 V)
- Low Operating Current (100 μA) in Green Mode
- Soft Start with 0 V / 6 V Gate Output Voltage
- Short Turn−on and Turn−off Delay Time (30 ns / 30 ns)
- High Gate Sourcing and Sinking Current (1.5 A / 4.5 A)
- Wide Operating Supply Voltage Range from 6.5 V to 35 V
- Wide Operating Frequency Range (22 kHz to 500 kHz)
- SOIC−8 and SOIC−8 EP Packages
- These Devices are Pb−Free and are RoHS Compliant

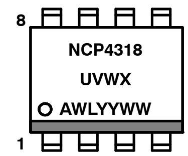
Applications

- High Power Density Adapters
- Large Screen LED−TV and OLED−TV Power Supplies
- High Efficiency Desktop and Server Power Supplies
- Networking and Telecom Power Supplies
- High Power LED Lighting

8

1
**SOIC−8 EP
CASE 751AC**

8

1
**SOIC−8, 150 mils
CASE 751BD**

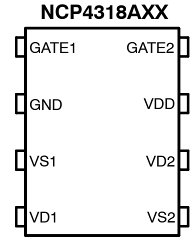
MARKING DIAGRAM



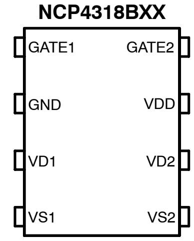
U = Pin Layout, A and B
V = Frequency, H: High, L: Low
WX = Additional IPT Option
A = Assembly Location
WL = Wafer Lot Traceability
YYWW = Date Code

PIN CONNECTIONS

NCP4318AXX



NCP4318BXX



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

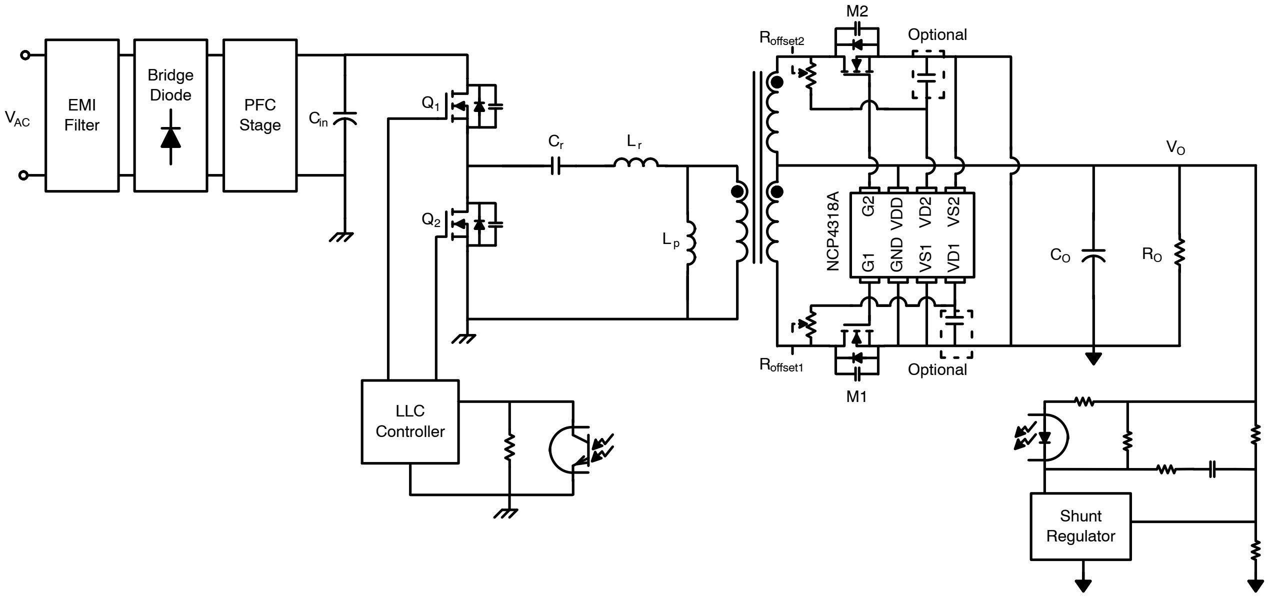


Figure 1. Typical Application Schematic of NCP4318

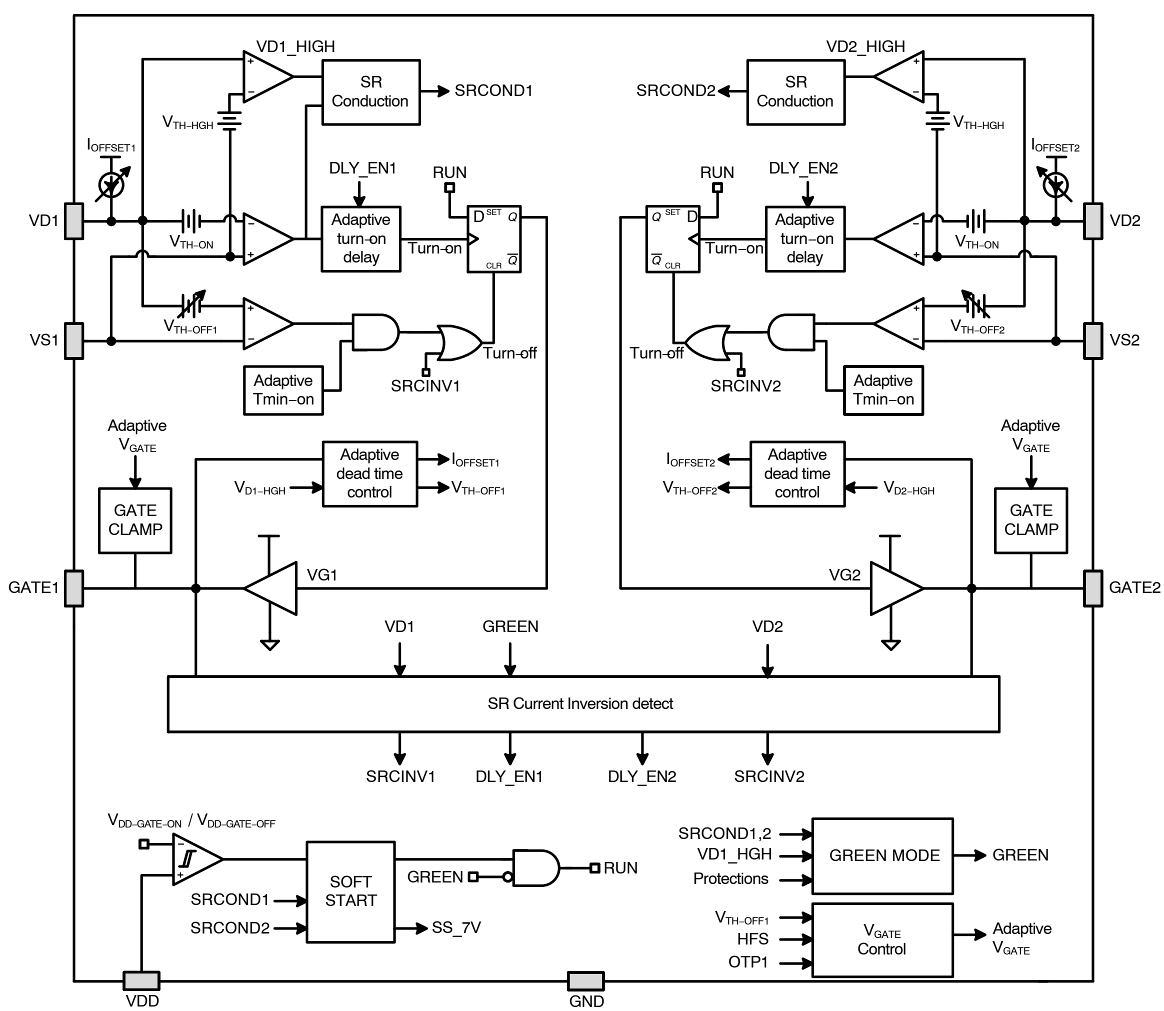


Figure 2. Internal Block Diagram of NCP4318

PIN DESCRIPTION

Pin Number		Name	Description
NCP4318A	NCP4318B		
1	1	GATE1	Gate drive output for SR MOSFET1
2	2	GND	Ground
3	4	VS1	Synchronous rectifier source sense input for SR1
4	3	VD1	Synchronous rectifier drain sense input. $I_{OFFSET1}$ current source flows out of the VD1 pin such that an external series resistor can be used to adjust the synchronous rectifier turn−off threshold. The $I_{OFFSET1}$ current source is turned off when V_{DD} is under−voltage or when switching is disabled in green mode
5	5	VS2	Synchronous rectifier source sense input for SR2
6	6	VD2	Synchronous rectifier drain sense input. $I_{OFFSET2}$ current source flows out of the VD2 pin such that an external series resistor can be used to adjust the synchronous rectifier turn−off threshold. The $I_{OFFSET2}$ current source is turned off when V_{DD} is under−voltage or when switching is disabled in green mode
7	7	VDD	Supply Voltage
8	8	GATE2	Gate drive output for SR MOSFET2

ORDERING INFORMATION

Ordering Code	Device Marking	Package	Shipping†
NCP4318AHDDR2G	NCP4318AHD	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4318AHJDR2G	NCP4318AHJ		
NCP4318ALCDR2G	NCP4318ALC		
NCP4318ALKDR2G	NCP4318ALK		
NCP4318ALSDR2G	NCP4318ALS		
NCP4318BLCDR2G	NCP4318BLC		
NCP4318ALFPDR2G‡	NCP4318ALFP	SOIC−8 EP (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
‡In development. Available upon request.

MAXIMUM RATINGS

Symbol	Rating		Value	Unit
V_{DD}	Power Supply Input Pin Voltage		−0.3 to 37	V
V_{D1}, V_{D2}	Drain Sense Input Pin Voltage		−4 to 200	V
V_{GATE1}, V_{GATE2}	Gate Drive Output Pin Voltage		−0.3 to 17	V
V_{S1}, V_{S2}	Source Sense Input Pin Voltage		−0.3 to 5.5	V
V_{S1-DYN}, V_{S2-DYN}	Source Sense Input Pin Dynamic Voltage (Pulse Width = 200 ns)		−4 to 5.5	V
P_D	Power Dissipation (T_A = 25°C) SOIC−8 SOIC−8 EP		 0.625 TBD	W
T_J	Maximum Junction Temperature		−40 to 150	°C
T_{STG}	Storage Temperature Range		−60 to 150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS−001−2012 (except VD1, VD2 pin)	3	kV
		Human Body Model, VD1−GND, VD2−GND pin to pin with 330−pF (Note 2) capacitance on VD1 and VD2 pin	2	
		Charged Device Model, JESD22−C101	1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values are with respect to the GND pin.
2. The capacitance can be replaced by C_{OSS} of MOSFET.

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient. SOIC−8 (Note 3) SOIC−8 EP (Note 4)	 165 40	°C/W
$R_{\psi JT}$	Thermal Characterization Parameter between Junction and the Center of the Top of the Package. SOIC−8 (Note 3) SOIC−8 EP (Note 4)	 22 4	°C/W

3. JEDEC standard: JESD51−2 (still air natural convection) and JESD51−3 (1s0p).
4. JEDEC standard: JESD51−2 (still air natural convection) and JESD51−7 (2s2p) with an additional 1−oz 1−in^2 copper spreader.

RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Min	Max	Unit
V_{DD}	VDD Pin Supply Voltage to GND (Note 5)	0	35	V
V_{D1}, V_{D2}	Drain Sense Input Pin Voltage	−0.7	180	V
V_{S1}, V_{S2}	Source Sense Input Pin Voltage	−0.3	5	V
T_J	Operating Junction Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Allowable operating supply voltage V_{DD} can be limited by the power dissipation of NCP4318 related to switching frequency, load capacitance and ambient temperature.

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to 125°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE AND CURRENT SECTION						
V_{DD-ON}	Turn−on Threshold	V_{DD} rising with 4.3 V / 1 ms	–	4.0	4.3	V
V_{DD-OFF}	Turn−off Threshold	$V_{DD} < V_{DD-OFF}$	3.6	3.8	–	V
$V_{DD-GATE-ON}$	SR Gate Enable Threshold Voltage	$V_{DD} > V_{DD-GATE-ON}$	–	6.5	7.1	V
$V_{DD-GATE-OFF}$	SR Gate Disable Threshold Voltage (Note 6)	$V_{DD} < V_{DD-GATE-OFF}$	5.0	6.0	–	V
I_{DD-OP1}	Operating Current	f_{SW} = 100 kHz, C_{GATE} = 1 nF	–	8	10	mA
I_{DD-OP0}	Operating Current	f_{SW} = 100 kHz, C_{GATE} = 0 nF	–	–	6	mA
$I_{DD-START}$	Start−up Current	$V_{DD} = V_{DD-ON}$ − 0.1 V	–	–	100	μA
$I_{DD-GREEN}$	Operating Current in Green Mode	V_{DD} = 12 V (no $V_{D1/2}$ switching) GREEN1 enable at T_J = 25°C	–	100	210	μA
$\eta_{SS-SKIP}$	Number of $V_{D1/2}$ Alternative Switching for Soft Start Skipping	$V_{D1/2}$ falling lower than V_{TH-ON} & $V_{D1/2}$ rising higher than V_{TH-HGH} & No GATE output at f_{SW} = 200 kHz, C_{GATE} = 0 nF	–	255	–	Cycle
DRAIN VOLTAGE SENSING SECTION						
V_{OSI}	Comparator Input Offset Voltage (Note 6)		−1	0	1	mV
$I_{DRAIN-LKG}$	Drain Pin Leakage Current	$V_{D1/2}$ = 200 V	–		1	μA
V_{TH-ON}	Turn−on Threshold (Note 6)	R_{OFFSET} = 0 Ω (includes comparator input offset voltage)	–	−100	–	mV
$t_{OFF-MIN}$	Minimum Off−time	From $V_{D1/2}$ higher than V_{TH-HGH} in ALC, ALK, BLC, ALFP in ALS in AHD, AHJ	 1400 450 750	 2000 800 1150	 2800 1150 1550	ns
t_{ON-DLY}	Turn−on Propagation Delay	Turn−on comparator delay From $V_{D1/2}$ = −0.2 to V_{GATE} = 1 V, when DLY_EN = 0	–	30	80	ns
$t_{ON-DLY2}$	Turn−on De−bounce Time when Additional Turn−on Delay is Enabled (Note 6)	Turn−on comparator delay From $V_{D1/2}$ = −0.2 to V_{GATE} = 1 V, when DLY_EN = 1. in AHD, AHJ, ALC, ALK, ALS, BLC, ALFP	–	240	–	ns
$t_{OFF-DLY}$	Turn−off Propagation Delay	Turn−off comparator delay From $V_{D1/2}$ = 0.6 to V_{GATE} = 5.7 V	–	30	80	ns
$V_{TH-OFF-MIN}$	Minimum Turn−off Threshold Voltage (Note 6)	R_{OFFSET} = 0 Ω (includes comparator input offset voltage) in ALC, ALK, ALS, BLC, ALFP in AHD, AHJ	 – –	 −6 −14	 – –	mV
$V_{TH-OFF-STEP}$	Step Size of Adaptive Turn−off Threshold Voltage (Note 6)	R_{OFFSET} = 0 Ω in AHD, AHJ, ALC, BLC, ALFP in ALK, ALS	 – –	 4 8	 – –	mV
$V_{TH-OFF-MAX}$	Maximum Turn−off Threshold Voltage (Note 6)	R_{OFFSET} = 0 Ω, in ALC, BLC, ALFP in ALK, ALS in AHD, AHJ	 – – –	 118 242 110	 – – –	mV
$V_{TH-OFF-RST}$	Reset Value of Turn−off Threshold Voltage (Note 6)	R_{OFFSET} = 0 Ω, in ALC, BLC, ALFP in ALK, ALS in AHJ	 – – –	 2 10 −10	 – – –	mV
$K_{2ND-VOFF}$	Ratio of Second−step V_{TH-OFF} to V_{TH-OFF} (Note 6)	LLD = 0. If LLD ≥ 1, 2nd step $V_{TH-OFF} = V_{TH-OFF}$	–	60	–	%
$K_{2ND-TOFF}$	Effective On−time Duration Ratio to On−time of Last Switching Cycle for the Second Step V_{TH-OFF} (Note 6)	LLD = 0, $t_{VG1}(n-1)$ = 8 μs, and $K_{2ND-TOFF} * t_{VG1}(n-1) > t_{MIN-ON}$. If $K_{2ND-TOFF} * t_{VG1}(n-1) < t_{MIN-ON}$, $t_{VG1-70} = t_{MIN-ON}$	–	70	–	%

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to 125°C unless otherwise specified.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN VOLTAGE SENSING SECTION						
V_{TH-HGH}	Drain Voltage High Detect Threshold Voltage (Note 6)	$V_{D1/2}$ rising in AHD, AHJ, ALC,ALK, BLC, ALFP in ALS	 – –	 0.85 1.5	 – –	V
$t_{GATE-SKIP1}$	Minimum SR Conduction Time to Enable SR when DLY_EN = 0 (3 Steps $V_{TH-OFF1\ or\ 2}$ Decrease when Gate Skip is Triggered)	The duration from turn−on trigger to $V_{D1/2}$ rising higher than V_{TH-HGH} ,when DLY_EN = 0 in ALC, ALK, ALS, BLC, ALFP in AHD, AHJ	 500 350	 710 550	 – –	ns
$t_{GATE-SKIP2}$	Minimum SR Conduction Time to Enable SR when DLY_EN = 1 (3 Steps $V_{TH-OFF1\ or\ 2}$ Decrease when Gate Skip is Triggered) (Note 6)	The duration from turn−on trigger to $V_{D1/2}$ rising higher than V_{TH-HGH} , when DLY_EN = 1 in ALC, ALK, ALS, BLC, ALFP in AHD, AHJ	 – –	 510 385	 – –	ns
MINIMUM ON−TIME AND MAXIMUM ON−TIME SECTION						
K_{TON1}	Adaptive Minimum On Time Ratio when DLY_EN = 0	DLY_EN=0 & $t_{SRCOND}(n-1)$ = 8 µs $t_{MIN-ON} = K_{TON1} * t_{SRCOND}(n-1)$	43	50	57	%
K_{TON2}	Adaptive Minimum On Time Ratio when DLY_EN = 1	DLY_EN=1 & $t_{SRCOND}(n-1)$ = 8 µs $t_{MIN-ON} = K_{TON2} * t_{SRCOND}(n-1)$	–	20	–	%
$t_{MIN-ON-U1}$	Upper Limit of Minimum On−time when DLY_EN = 0	200 ns < t_{MIN-ON} < $t_{MIN-ON-U1}$, DLY_EN = 0	4	5	6	µs
$t_{MIN-ON-U2}$	Upper Limit of Minimum On−time when DLY_EN = 1	200 ns < t_{MIN-ON} < $t_{MIN-ON-U2}$, DLY_EN = 1	2	2.5	3	µs
K_{INV1}	SR Current Inversion Detection Window Ratio when DLY_EN = 0	$K_{TON1} = K_{INV1}$, DLY_EN = 0 $t_{INV-WIN} = t_{MIN-ON}$	43	50	57	%
K_{INV2}	SR Current Inversion Detection Window Ratio when DLY_EN = 1	$K_{TON2} = K_{INV2}$, DLY_EN = 1 $t_{INV-WIN} = t_{MIN-ON}$	–	20	–	%
$\eta_{INV-EXT}$	Consecutive Normal Switching Cycles to Exit SR Current Inversion State DLY_EN = 1 (Note 6)	Without parasitic $V_{D1/2}$ oscillation	–	16k	–	cycle
$t_{SR-MAX-ON}$	Maximum SR Turn−on Time (Note 6)	in none in ALC, ALK, ALS, AHD, AHJ, BLC, ALFP	21 –	30 Inf.	39 –	µs
f_{MIN}	Minimum Switching Frequency (Note 6)	$1 / (t_{SR-MAX-ON-CH1} + t_{SR-MAX-ON-CH2})$ in none in ALC, ALK, ALS, AHD, AHJ, BLC, ALFP	 – –	 – –	 22 0	kHz
DEAD TIME REGULATION SECTION						
I_{OFFSET}	Maximum of Adaptive Offset Current which have 31 Steps and 10 µA of Resolution	$V_{D1} = V_{D2} = 0$	285	310	335	µA
$t_{DEAD-LBAND}$	Lower Band of Dead Time Regulation (Note 6)	From V_{GATE} falling below $V_{GATE-LOW}$ in ALC, ALK, ALS, BLC, ALFP in AHD, AHJ	 – –	 90 170	 – –	ns
$t_{DEAD-HBAND}$	Upper Band of Dead Time Regulation (Note 6)	From V_{GATE} falling below $V_{GATE-LOW}$, when LLD = 0	–	$t_{DEAD-LBAND}$ + 90	–	ns
η_{LLD1}	First Light Load Detection (LLD1) Step Number based on V_{TH-OFF} Modulator (Note 6)	$\eta V_{TH-OFF-CNT} \leq \eta_{LLD1}$	–	7	–	
η_{LLD2}	Second Light Load Detection (LLD2) Step Number based on V_{TH-OFF} Modulator (Note 6)	$\eta V_{TH-OFF-CNT} \leq \eta_{LLD2}$	–	3	–	

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to 125°C unless otherwise specified.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
GREEN MODE SECTION						
$t_{GRN1-ENT}$	Non−switching Period of SR Gate to Enter Green Mode	When SRCOND1, 2 are both low for $t_{GRN1-ENT}$, GREEN1 = HIGH. in ALC, ALK, ALS, BLC, ALFP in AHD, AHJ	 45 25	 60 40	 75 55	μs
$t_{GRN2-ENT}$	Non−switching Period of SR Gate to Reset V_{TH-OFF} and Set DLY_EN	When SRCOND1, 2 are both low for $t_{GRN2-ENT}$, generate GREEN2 pulse. in ALC, ALK, ALS, BLC, ALFP in AHD, AHJ	 4.5 2.5	 6 4	 7.5 5.5	μs
$\eta_{CSW-EXT}$	Number of Buffer Switching Cycle to Recover I_{DD-OP} when IC Exits from Green mode	Number of switching with V_{D1} > V_{TH-HGH} to exit GREEN1	–	4	–	cycle
PROTECTION SECTION						
V_{SRCINV}	Threshold Voltage of Current Inversion Detection (Note 6)	LLD = 0 LLD ≥ 1, Virtual V_{TH-OFF}	– –	0 V_{TH-OFF}	– –	mV
t_{INV}	Debounce Time of SR Current Inversion Detection (Note 6)	$V_{GATE1/2}$ > 4.5 V & $V_{D1/2}$ > V_{SRCINV} for t_{INV} in ALC, ALK, BLC, ALFP in ALS in AHD, AHJ	 – – –	 320 520 170	 – – –	ns
V_{SD-PRI}	Drain Threshold Voltage for Primary Shutdown Protection (Note 6)	$V_{GATE1/2}$ > 4.5 V with 200−ns delay & $V_{D1/2}$ > V_{SD-PRI} when DLY_EN = 0. $V_{GATE1/2}$ > 4.5V with 100−ns delay & $V_{D1/2}$ > V_{SD-PRI} when DLY_EN = 1. in ALC, ALK, BLC, ALFP in ALS in AHD, AHJ	 – – –	 150 200 100	 – – –	mV
K_{SD-PRI}	Detection Window Time Ratio Based on t_{VG1}(n−1) for the Primary Shutdown Protection (Note 6)	LLD = 0, t_{VG1}(n−1) = 8 μs, and $K_{2ND-TOFF}$ * t_{VG1}(n−1) > t_{MIN-ON}. If $K_{2ND-TOFF}$ *t_{VG1}(n−1) < t_{MIN-ON}, t_{VG1-70} = t_{MIN-ON}.	65	70	75	%
V_{ABN-VD}	Drain Threshold Voltage to Trigger Abnormal VD Sensing Protection (Note 6)	$V_{D1/2}$ > V_{ABN-VD} & $V_{GATE1/2}$ > 4.5 V with 100−ns delay within K_{SD-PRI}. V_{ABN-VD} = V_{TH-HGH} in AHD, AHJ, ALC,ALK, BLC, ALFP in ALS	 – –	 0.85 1.5	 – –	V
T_{OTP1}	Over Temperature Protection Reducing V_{GATE} (Note 6)	T_J > T_{OTP1} & V_{GATE}=6.7V in AHJ, ALC, BLC, ALFP in AHD, ALK, ALS	 – –	 105 130	 – –	°C
T_{OTP2}	Over Temperature Protection Stopping Gate Operation (Note 6)	T_J > T_{OTP2} & No gate output in AHJ, ALC, BLC, ALFP in AHD, ALK, ALS	 – –	 140 disable	 – –	°C
$T_{OTP-RST}$	Reset Level of Over Temperature Protection (Note 6)	T_J < $T_{OTP-RST}$, OTP1 and OTP2 are reset	–	80	–	°C
GATE DRIVER SECTION						
$V_{GATE-MAX}$	Gate Clamping Voltage (Note 6)	12 V < V_{DD} < 33 V, C_{GATE} = 4.7 nF at T_J < T_{OTP1}	9	10.5	12	V
$V_{GATE-MAX-6V}$	Gate Clamping Voltage for Adaptive Gate Voltage Control (Note 6)	V_{DD} = 12 V, C_{GATE} = 4.7 nF in ALC, BLC	5.0	6.7	8.2	V
t_{HFS-EN}	Adaptive Gate Control Enabling Switching Period (Note 6)	The time duration from V_{GATE1}(n−1) rising edge to V_{GATE1}(n) rising edge at T_J<T_{OTP1}. in ALC, ALK, ALS, BLC, ALFP in AHD, AHJ	 4 –	 5 4	 6.1 –	μs
I_{SOURCE}	Peak Sourcing Current of Gate Driver (Note 6)		–	1.5	–	A
I_{SINK}	Peak Sinking Current of Gate Driver (Note 6)		–	4.5	–	A

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to 125°C unless otherwise specified.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
GATE DRIVER SECTION						
$R_{DRV-SOURCE}$	Gate Driver Sourcing Resistance (Note 6)		–	8	–	Ω
$R_{DRV-SINK}$	Gate Driver Sinking Resistance (Note 6)		–	1.5	–	Ω
t_R	Rise Time	V_{DD} = 12 V, C_{GATE} = 3.3 nF, V_{GATE} = 1 → 6 V at T_J = 25°C	–	50	150	ns
t_F	Fall Time	V_{DD} = 12 V, C_{GATE} = 3.3 nF, V_{GATE} = 6 → 1 V at T_J = 25°C	–	30	50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Not tested but guaranteed by design

IC OPTIONS

Option	Drain Sensing Pin	Frequency	DLY_EN	VGATE	$t_{GATE-LIM}$	T_{OTP1} / T_{OTP2}
NCP4318ALC	#4, #6	L–version	Variable	2–Level (10V, 6V)	Disabled	105°C / 140°C
NCP4318BLC	#3, #6	L–version	Variable	2–Level (10V, 6V)	Disabled	105°C / 140°C
NCP4318ALS	#4, #6	L–version	Always High	1–Level (10V)	Disabled	130°C / Disable
NCP4318AHD	#4, #6	H–version	Variable	1–Level (10V)	Disabled	130°C / Disable
NCP4318AHJ	#4, #6	H–version	Variable	1–Level (10V)	Disabled	105°C / 140°C
NCP4318ALK	#4, #6	L–version	Variable	1–Level (10V)	Disabled	130°C / Disable
NCP4318ALFP	#4, #6	L–version	Variable	1–Level (10V)	Disabled	105°C / 140°C

Option	t_{INV} (ns)	$t_{DEAD-LBAND}$ (ns)	$t_{OFF-MIN}$ (μs)	$t_{GATE-SKIP1}$ (ns) / $t_{GATE-SKIP2}$ (ns)	$t_{GRN1-ENT}$ (μs) / $t_{GRN2-ENT}$ (μs)	f_{HFS-EN} (kHz)
NCP4318ALC	320	90	2	710 / 510	60 / 6	200
NCP4318BLC	320	90	2	710 / 510	60 / 6	200
NCP4318ALS	520	90	0.8	710 / 510	60 / 6	200
NCP4318AHD	170	170	1.15	550 / 385	40 / 4	250
NCP4318AHJ	170	170	1.15	550 / 385	40 / 4	250
NCP4318ALK	320	90	2	710 / 510	60 / 6	200
NCP4318ALFP	320	90	2	710 / 510	60 / 6	200

Option	V_{TH-HGH} (V)	V_{TH-OFF} Range (mV)	$V_{TH-OFF-STEP}$ (mV)	$V_{TH-OFF-RST}$ (mV)	V_{SD-PRI} (mV)
NCP4318ALC	0.85	−6 ~ 118	4	2	150
NCP4318BLC	0.85	−6 ~ 118	4	2	150
NCP4318ALS	1.5	−6 ~ 242	8	10	200
NCP4318AHD	0.85	−14 ~ 110	4	−10	100
NCP4318AHJ	0.85	−14 ~ 110	4	−10	100
NCP4318ALK	0.85	−6 ~ 242	8	10	150
NCP4318ALFP	0.85	−6 ~ 118	4	2	150

7. f_{HFS-EN} = 1 / t_{HFS-EN}.

TYPICAL PERFORMANCE CHARACTERISTICS

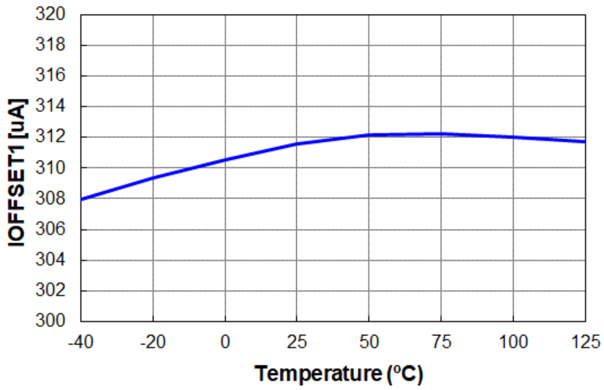


Figure 3. $I_{OFFSET1}$ vs. Temperature

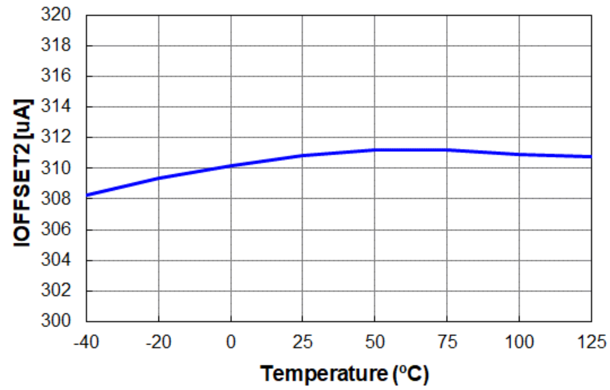


Figure 4. $I_{OFFSET2}$ vs. Temperature

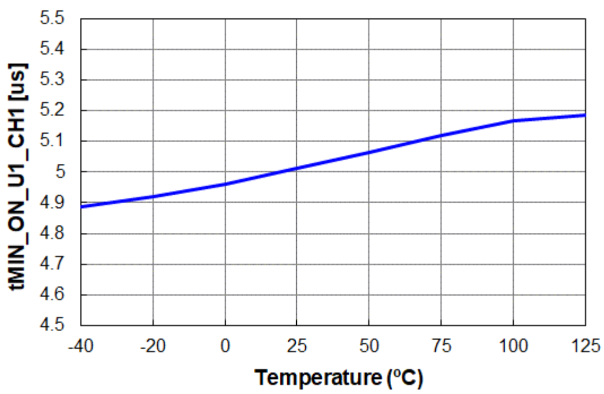


Figure 5. $t_{MIN-ON-U1-CH1}$ vs. Temperature

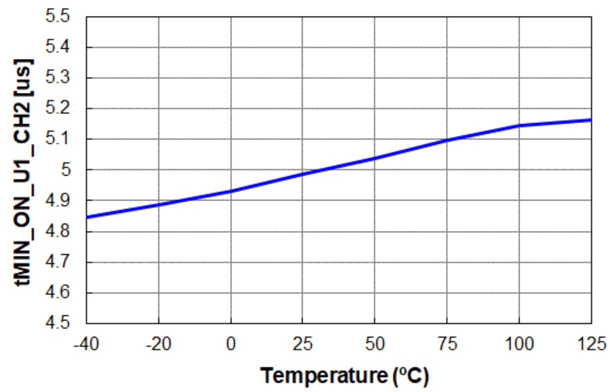


Figure 6. $t_{MIN-ON-U1-CH2}$ vs. Temperature

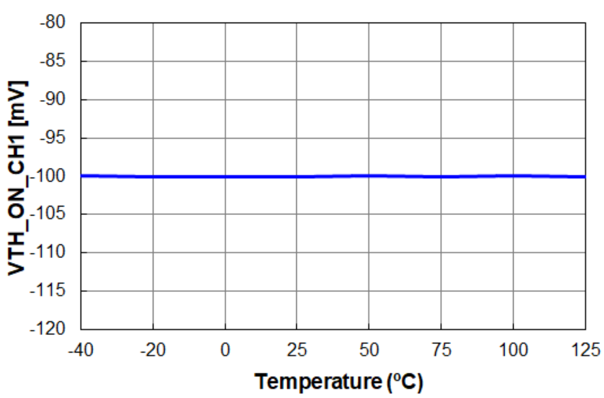


Figure 7. $V_{TH-ON-CH1}$ vs. Temperature

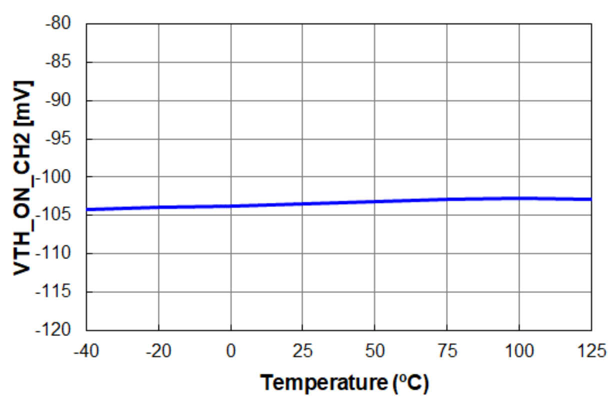


Figure 8. $V_{TH-ON-CH2}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

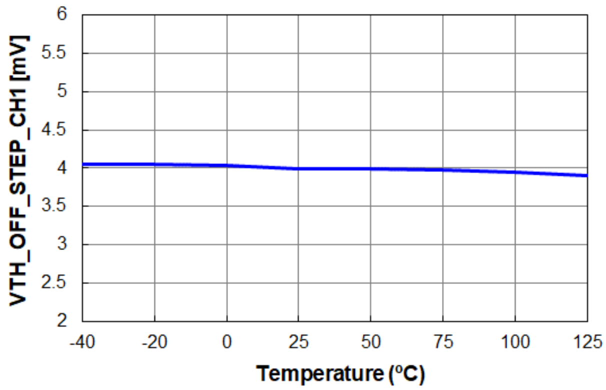


Figure 9. $V_{TH-OFF-STEP-CH1}$ vs. Temperature

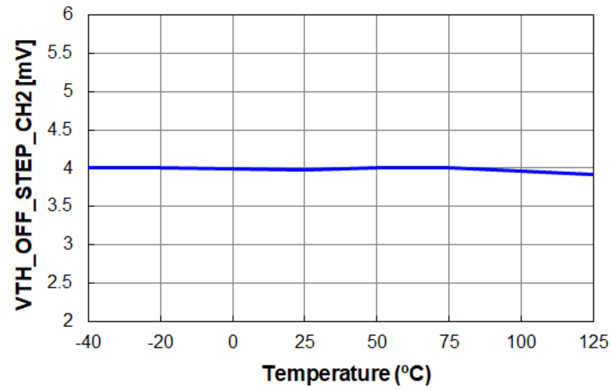


Figure 10. $V_{TH-OFF-STEP-CH2}$ vs. Temperature

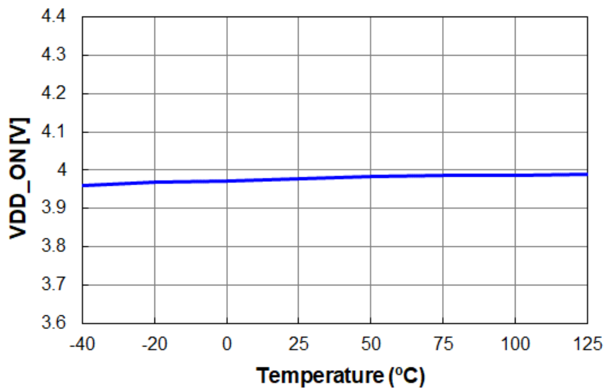


Figure 11. V_{DD-ON} vs. Temperature

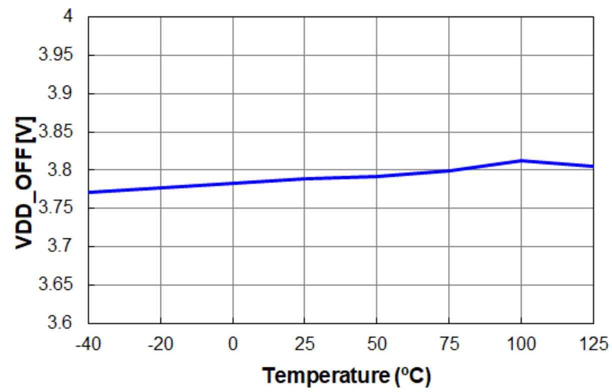


Figure 12. V_{DD-OFF} vs. Temperature

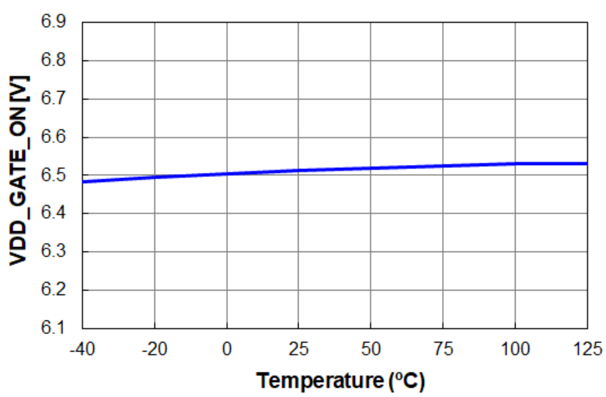


Figure 13. $V_{DD-GATE-ON}$ vs. Temperature

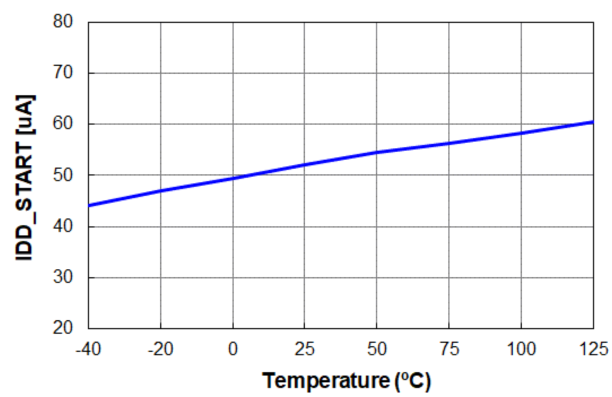


Figure 14. $I_{DD-START}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

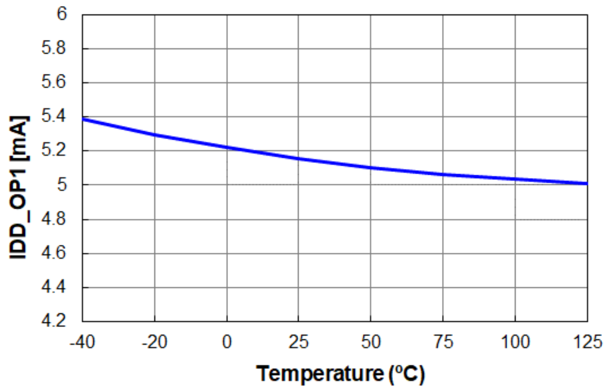


Figure 15. I_{DD-OP1} vs. Temperature

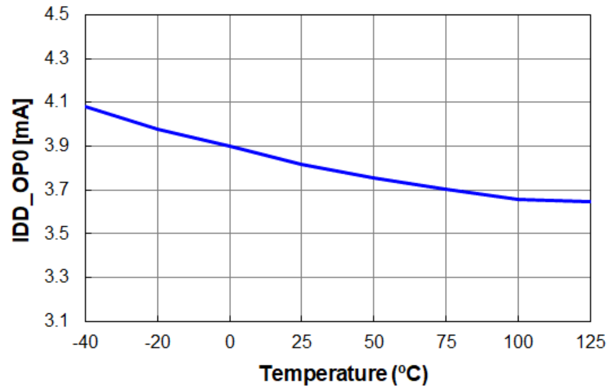


Figure 16. I_{DD-OP0} vs. Temperature

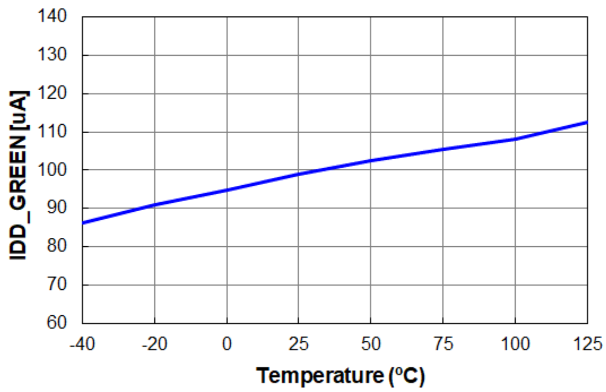


Figure 17. $I_{DD-GREEN}$ vs. Temperature

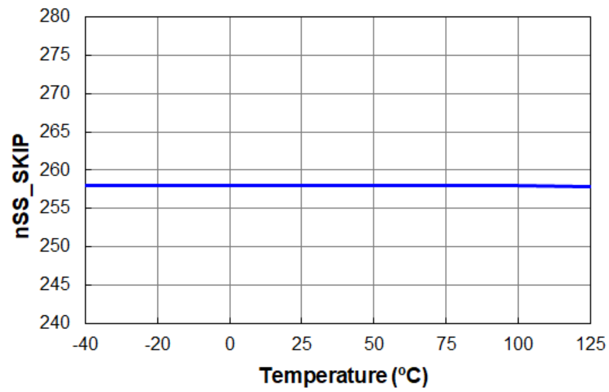


Figure 18. $n_{SS-SKIP}$ vs. Temperature

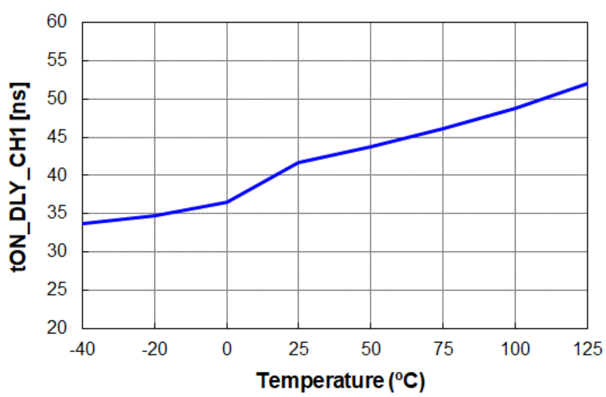


Figure 19. $t_{ON-DLY-CH1}$ vs. Temperature

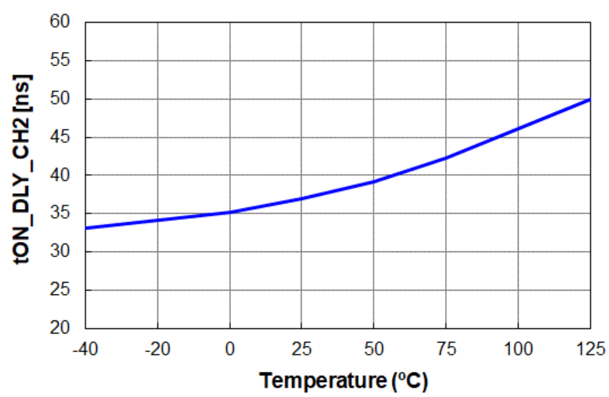


Figure 20. $t_{ON-DLY-CH2}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

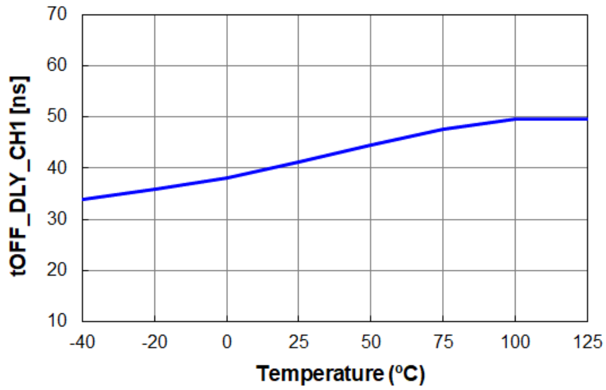


Figure 21. $t_{OFF-DLY-CH1}$ vs. Temperature

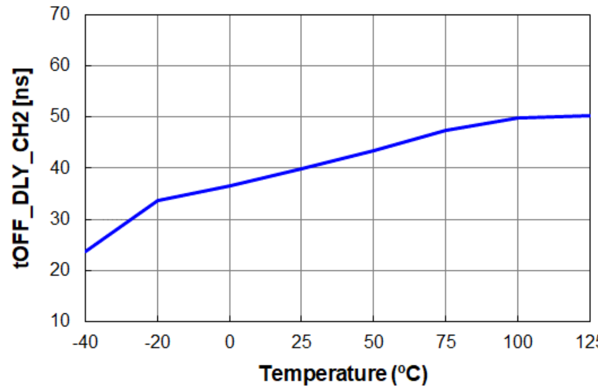


Figure 22. $t_{OFF-DLY-CH2}$ vs. Temperature

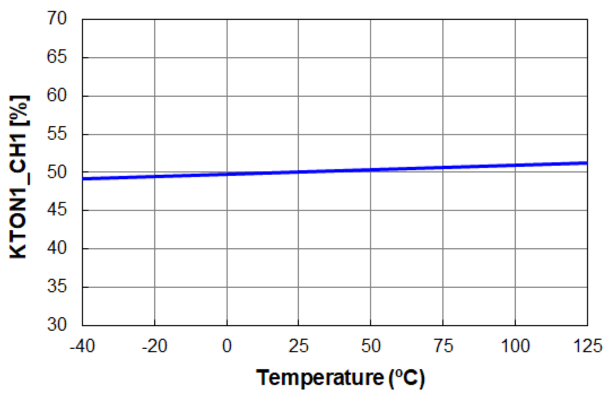


Figure 23. $K_{TON1-CH1}$ vs. Temperature

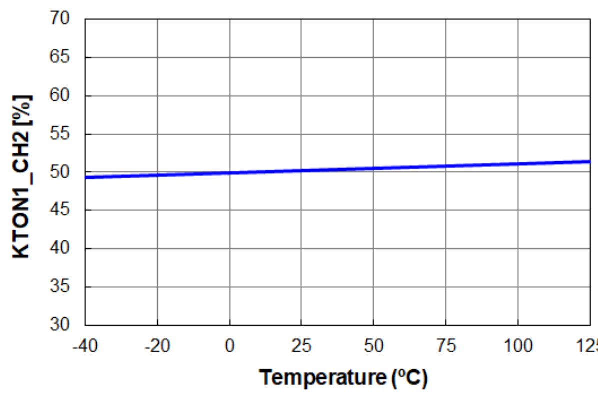


Figure 24. $K_{TON1-CH2}$ vs. Temperature

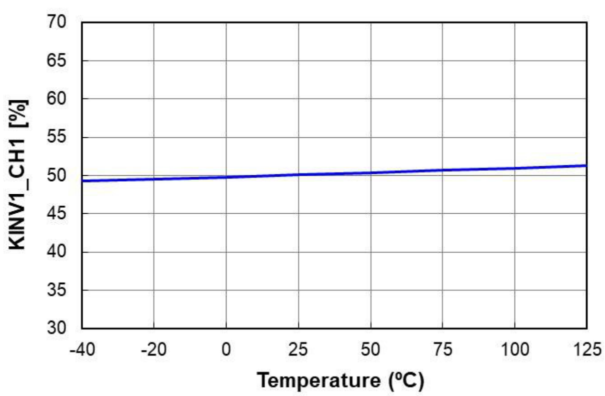


Figure 25. $K_{INV1-CH1}$ vs. Temperature

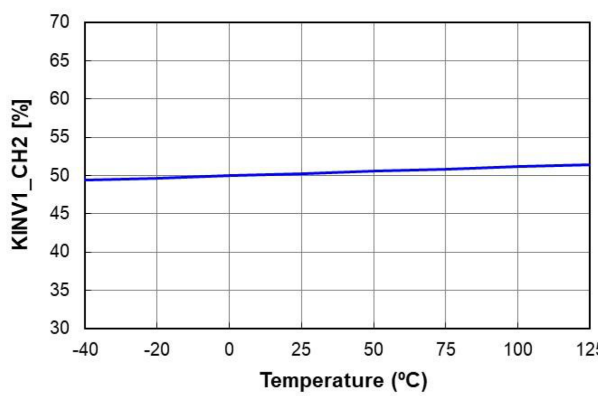


Figure 26. $K_{INV1-CH2}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

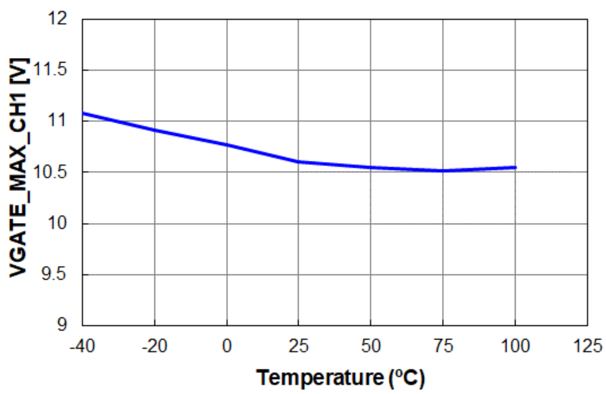


Figure 27. $V_{GATE-MAX-CH1}$ vs. Temperature

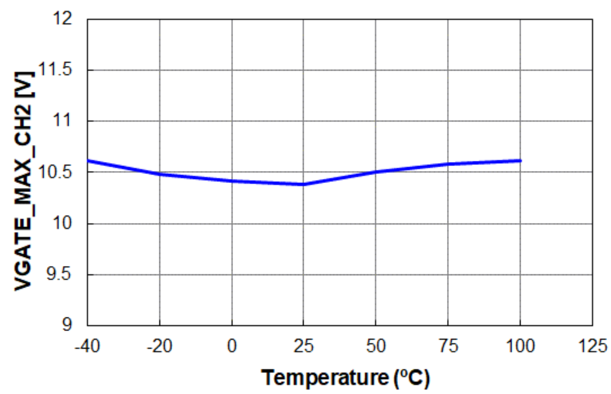


Figure 28. $V_{GATE-MAX-CH2}$ vs. Temperature

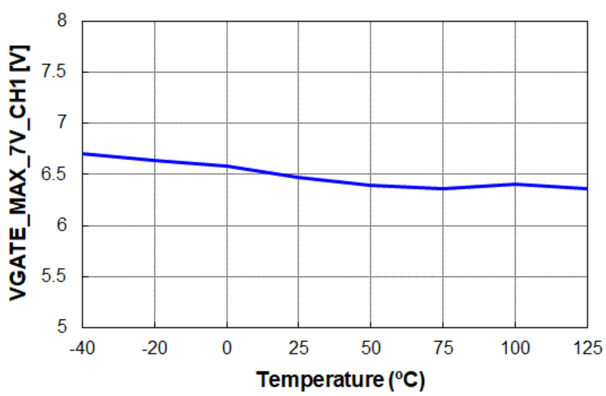


Figure 29. $V_{GATE-MAX-7V-CH1}$ vs. Temperature

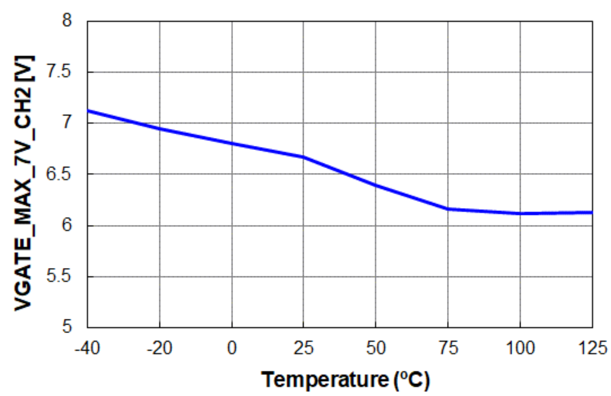


Figure 30. $V_{GATE-MAX-7V-CH2}$ vs. Temperature

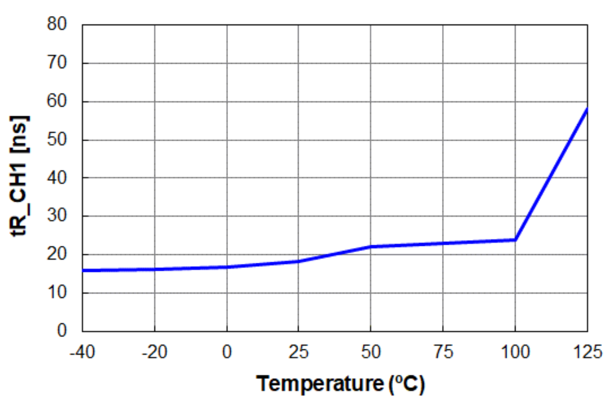


Figure 31. t_{R-CH1} vs. Temperature

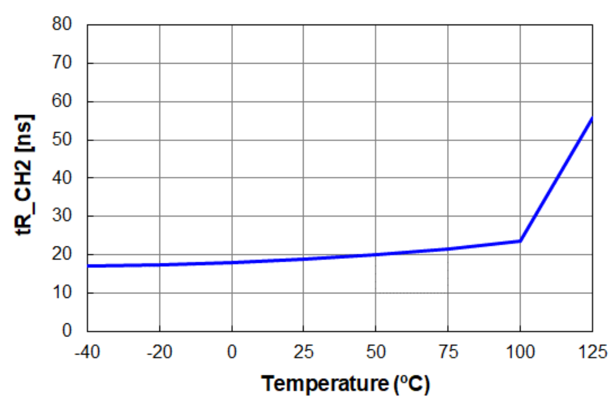


Figure 32. t_{R-CH2} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

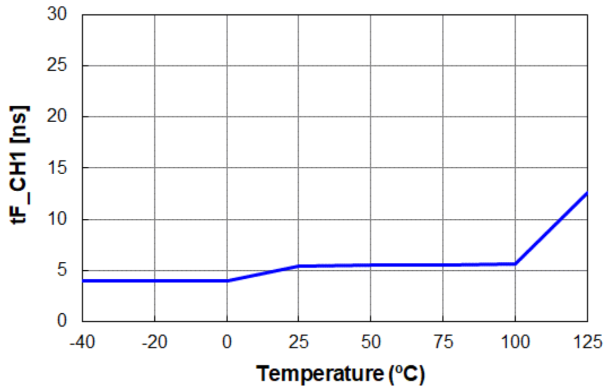


Figure 33. t_{F-CH1} vs. Temperature

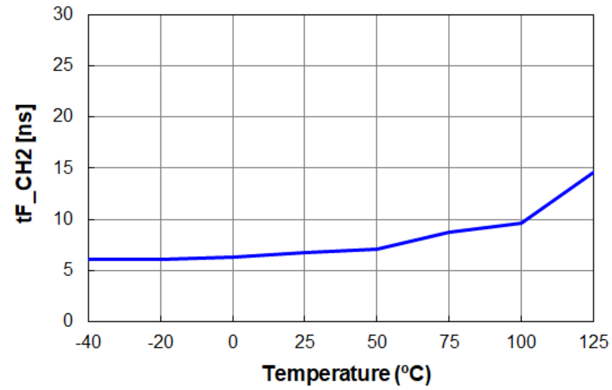


Figure 34. t_{F-CH2} vs. Temperature

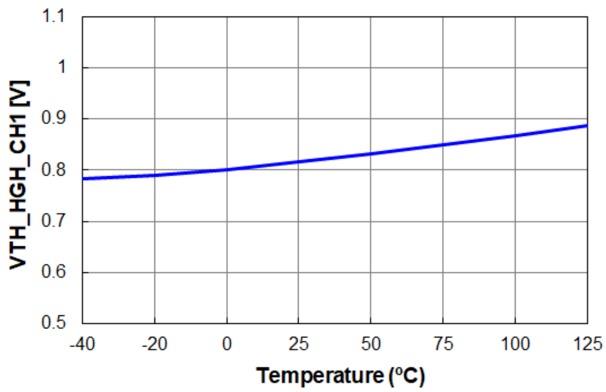


Figure 35. $V_{TH-HIGH-CH1}$ vs. Temperature

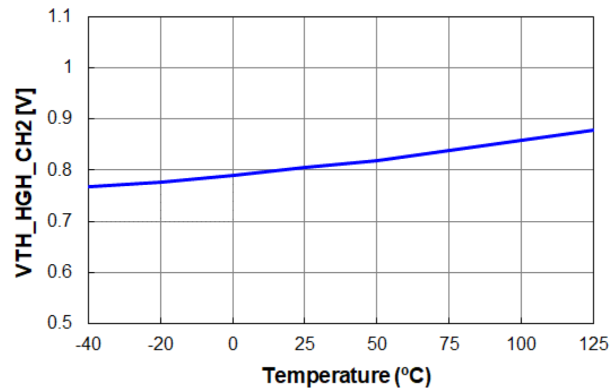


Figure 36. $V_{TH-HIGH-CH2}$ vs. Temperature

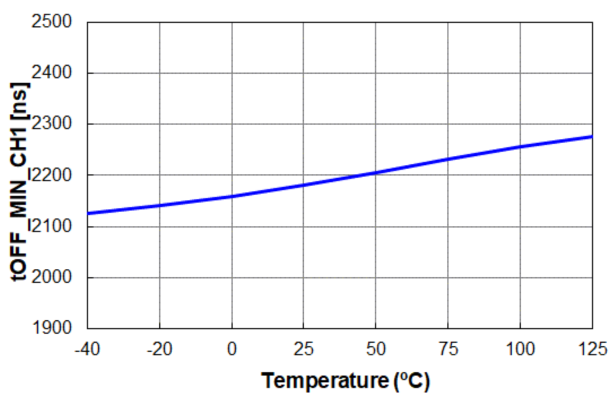


Figure 37. $t_{OFF-MIN-CH1}$ vs. Temperature

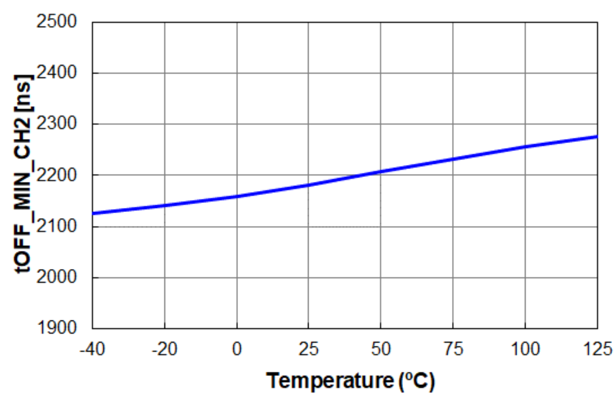


Figure 38. $t_{OFF-MIN-CH2}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

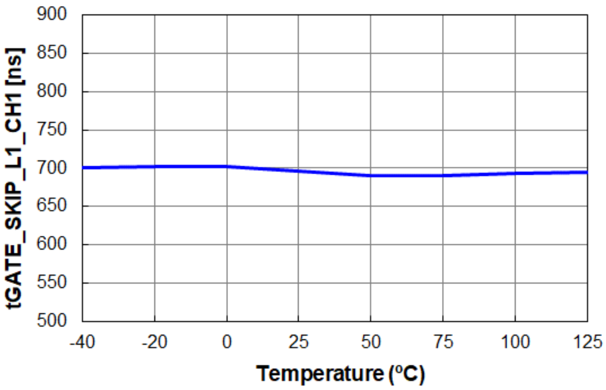


Figure 39. $t_{GATE-SKIP1-CH1}$ vs. Temperature

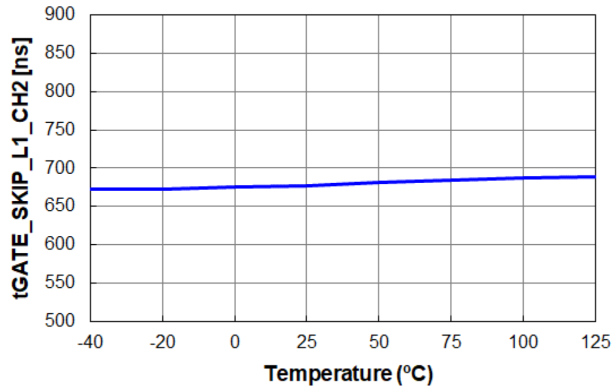


Figure 40. $t_{GATE-SKIP1-CH2}$ vs. Temperature

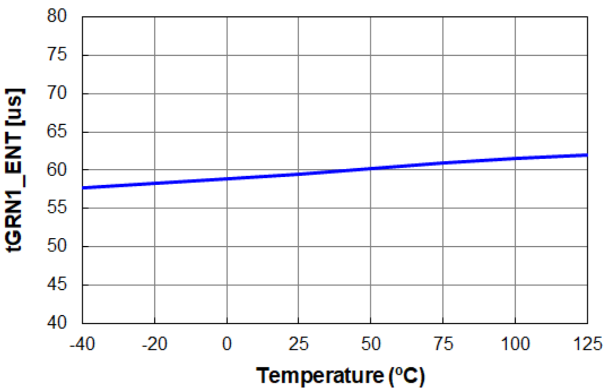


Figure 41. $t_{GRN1-ENT}$ vs. Temperature

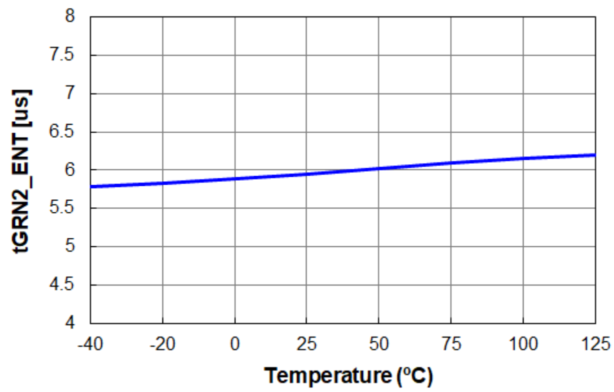


Figure 42. $t_{GRN2-ENT}$ vs. Temperature

APPLICATIONS INFORMATION

Basic Operation Principle

NCP4318 controls the SR MOSFETs based on the instantaneous drain−to−source voltage sensed across the drain and source pins of the MOSFET. Before SR gate turning on, SR body diode operates as the conventional diode rectifier. Referring to Figure 46, the conducting body diode makes the drain−to−source voltage drops below the turn−on threshold voltage V_{TH-ON} and triggers the turn−on of the SR gate. After the SR gate turning on, the product of on resistance R_{DS-ON} of the SR MOSFET and the instantaneous SR current determines the drain−to−source voltage.

When the drain−to−source voltage reaches the turn−off threshold voltage V_{TH-OFF}, as SR MOSFET current decreases to near zero, NCP4318 turns off the gate. If SR dead time is larger or smaller than the dead time regulation target, NCP4318 adaptively changes a virtual turn−off threshold voltage to regulate the dead time between $t_{DEAD-LBAND}$ and $t_{DEAD-HBAND}$, so to maximize system efficiency.

SR Turn−on Algorithm

When V_D is lower than V_{TH-ON} by body diode conduction of SR MOSFET, turn−on comparator *COM1* toggles high. If an additional delay flag signal *DLY_EN* is low, VG goes high with only 30 ns of t_{ON-DLY} and GATE sources 1.5 A of I_{SOURCE} to turn on the SR MOSFET.

On the other hand, if the *DLY_EN* flag is HIGH due to current inversion detection *SRCINV* or green−mode preparation *GREEN2*, additional turn−on delay is applied by an adaptive turn−on delay block. In this case, SR gate is turned on when the body diode conduction time is confirmed to be longer than $t_{ON-DLY2}$.

SR Turn−off Algorithm

The SR turn−off method determines safe and stable SR operation. One of the conventional methods turns off the SR gate based on the instantaneous drain voltage (present information). This method is widely used and easy to realize, and it can prevent late turn−off with appropriate turn−off threshold voltage. However, it frequently shows premature turn−off due to parasitic stray inductances of PCB trace and package of the SR MOSFET. On the other hand, SR gate on−time is predicted by inspecting previous−cycle drain voltage information. It can prevent the premature turn−off, providing good performance for the system with constant operating frequency and SR conduction duration. However, in case of the frequency changing, the on−time prediction may lead to late turn−off during frequency increasing event, leading to negative current flowing in the secondary side of the LLC converter.

To gain the advantages of both methods, NCP4318 adopts a mixed type turn−off algorithm, which modulate a virtual turn−off threshold voltage (V_{TH-OFF}) to regulate the turn−off dead time within a hysteresis band. As shown in Figure 45, the instantaneous drain voltage V_D is compared with a virtual V_{TH-OFF} to turn off the SR gate. The virtual V_{TH-OFF} is adaptively changed to compensate the effect of stray inductance and regulate a t_{DEAD} between $t_{DEAD-LBAND}$ and $t_{DEAD-HBAND}$. Therefore, NCP4318 can show robust operation with very small dead time

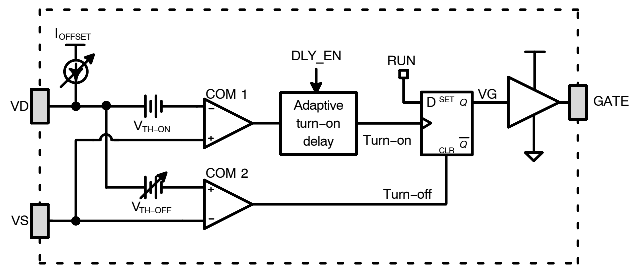


Figure 43. VDS−sensing Circuit

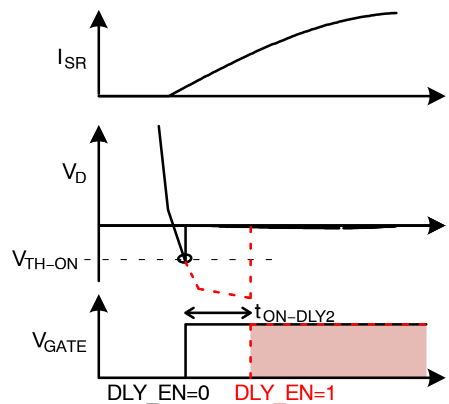


Figure 44. SR Turn−on Algorithm

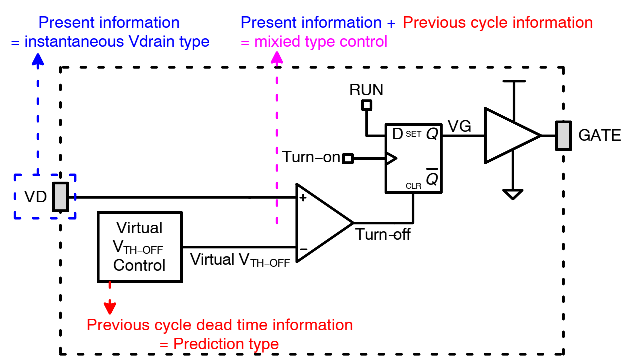


Figure 45. SR Turn−off Algorithm

Hysteresis−Band Dead−Time Regulation

The stray inductance of SR MOSFET induces a positive offset voltage across drain and source when the SR current decreases. This makes drain−to−source voltage of SR MOSFET higher than the product of R_{DS-ON} and the instantaneous SR current, which results in premature SR turn−off as shown in Figure 46 (a). The induced offset voltage changes as the output load varying, so, to keep a fixed SR dead time, the turn−off threshold voltage needs to be tuned. NCP4318 utilizes the virtual V_{TH-OFF}, which is comprised of 31 steps of turn−off threshold voltages $V_{TH-OFF(n)}$ and 31 steps of offset current $I_{OFFSET(n)}$ as shown in Figure 46 (b) and Figure 47. The turn−off condition and the virtual turn−off threshold voltage can be expressed as:

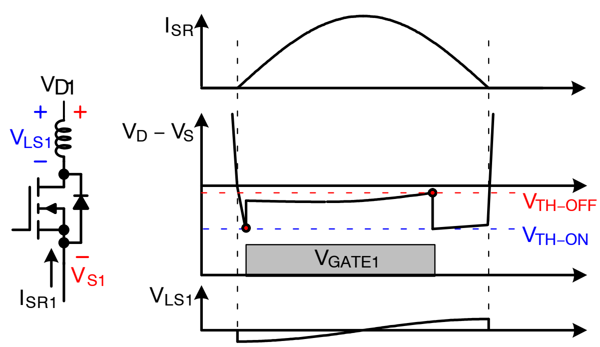
$$V_{DS} + I_{OFFSET} \cdot R_{OFFSET} - V_{TH-OFF} = 0 \qquad \text{(eq. 1)}$$

$$\text{Virtual } V_{TH-OFF} = V_{TH-OFF} - R_{OFFSET} \cdot I_{OFFSET} \qquad \text{(eq. 2)}$$

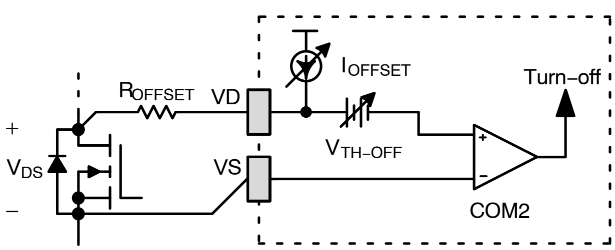
where R_{OFFSET} is the external drain sensing resistance.

V_{TH-OFF} modulates between $V_{TH-OFF-MIN}$ and $V_{TH-OFF-MAX}$ with a step size of $V_{TH-OFF-STEP}$, and I_{OFFSET} varies between 0 and 310 μA with 10 μA of step size. I_{OFFSET} means to provide a finer tuning on the virtual V_{TH-OFF}. When the I_{OFFSET} has saturated to maximum or minimum values, V_{TH-OFF} changes to its next step for a coarse control. So, designing the R_{OFFSET} resistance as $V_{TH-OFF-STEP}$ / 310 μA gives a linear virtual V_{TH-OFF} sweeping range. Typically, 30−Ω R_{OFFSET} is used when $V_{TH-OFF-STEP}$ is 8 mV, and 15 Ω for 4 mV.

Dead time is defined as the duration from V_{GATE} turning off to V_D exceeding V_{TH-HGH}. In Figure 48 (a), the measured dead time t_{DEAD} is larger than upper band of $t_{DEAD-HBAND}$. To reduce t_{DEAD}, the virtual V_{TH-OFF} will increased by one−step decrease of I_{OFFSET} within 128 switching cycles. As a result, t_{DEAD} decreases and becomes much closer to $t_{DEAD-HBAND}$, as shown in Figure 46 (b).



(a) Premature SR Turn−off by Stray Inductance



(b) Detailed SR Turn−off Circuitry

Figure 46. Virtual V_{TH-OFF}

Similarly, when the dead time is shorter than $t_{DEAD-LAND}$, the virtual V_{TH-OFF} will reduce in the following switching cycle. When the dead time is placed between $t_{DEAD-LBAND}$ and $t_{DEAD-HBAND}$ as in Figure 49, the virtual V_{TH-OFF} stays as−is. Therefore, the dead time is regulated between $t_{DEAD-LBAND}$ and $t_{DEAD-HBAND}$ regardless of parasitic inductances. This hysteresis−band dead−time control provides stable operation across load variation by minimizing the variation of the dead time.

The initial and reset condition of the virtual V_{TH-OFF} is $V_{TH-OFF} = V_{TH-OFF-RST}$ and I_{OFFSET} = 310 μA.

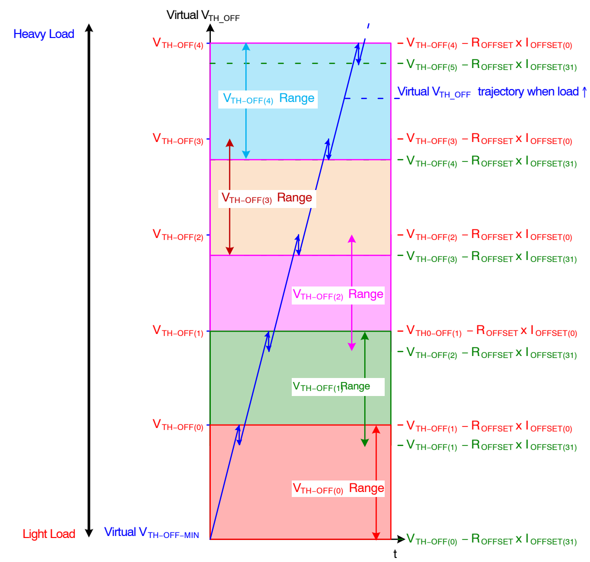
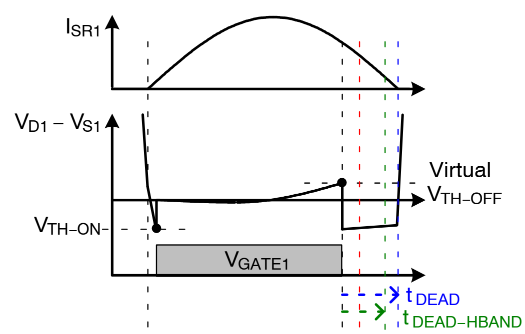
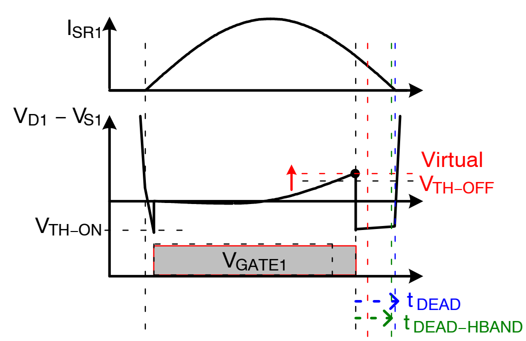


Figure 47. Virtual V_{TH-OFF} Trajectory when Load Increases



(a) $t_{DEAD} > t_{DEAD-HBAND}$



(b) $t_{DEAD} \approx t_{DEAD-HBNAD}$

Figure 48. Dead−time Regulation

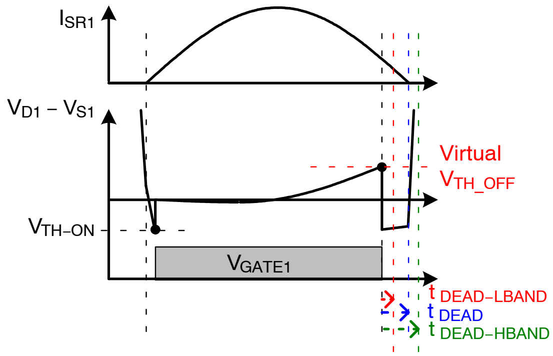


Figure 49. $t_{DEAD} \in [t_{DEAD-LBAND}, t_{DEAD-HBAND}]$

Light Load Detection (LLD)

When the output load increases, due to larger current amplitude in the SR current, the dead−time regulation modulates the V_{TH-OFF} higher. Thus, the V_{TH-OFF} indicates the output load condition.

There are totally 31 steps of V_{TH-OFF}, noted as $V_{TH-OFF(0)}$~$V_{TH-OFF(31)}$. When the output load increases, by the dead−time regulation, V_{TH-OFF} tends to increase. When V_{TH-OFF}'s step number $n \le \eta_{LLD1}$ on channel 1, NCP4318 detects a light load condition. So, light load detection flag signal *LLD* set to '1'. When the load keeps reducing, making $n \le \eta_{LLD2}$, *LLD* is set to '2'. At heavier load and $n > \eta_{LLD1}$, *LLD* becomes '0'. This *LLD* signal is used for *SRCINV* detection threshold voltage control and adaptive V_{GATE} control.

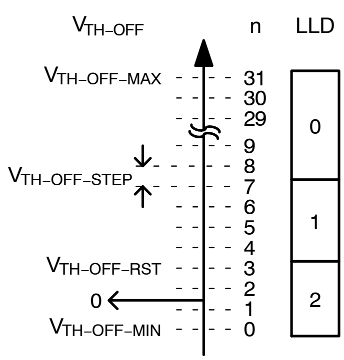


Figure 50. V_{TH-OFF} Steps and the LLD Flag (η_{LLD1} = 7, η_{LLD2} = 3, $\eta_{VTH-OFF-RST}$ = 3)

Advanced Adaptive Minimum Turn−on Time

When SR gate is turning on, there may be severe oscillation in the drain−to−source voltage of the SR MOSFET, which may result in several turn−off mis−triggering as shown in Figure 51. To provide stable SR gate signal without short pulses, it is desirable to have large turn−off blanking time (= minimum turn−on time) until the drain voltage oscillation attenuates. However, too large blanking time results in an inversion current problem under light load condition where the SR conduction time may be shorter than the minimum turn−on time.

To solve this issue, NCP4318 has an adaptive minimum turn−on time, t_{MIN-ON}, where the turn−off blanking time changes in accordance with the SR conduction time t_{SRCOND}(n−1) measured in previous switching cycle. The SR conduction time is measured from SR gate rising edge to the drain sensing voltage V_D being higher than V_{TH-HGH}. t_{MIN-ON} in the n−th switching cycle is defined as 50% of t_{SRCOND}(n−1) as shown in Figure 52. During t_{MIN-ON}, SR gate won't be turned off by the virtual V_{TH-OFF}. The minimum and maximum values of t_{MIN-ON} are defined as 200 ns and $t_{MIN-ON-U1}$ respectively. When the additional turn−on delay flag *DLY_EN* is high in the light load condition, t_{MIN-ON} becomes 20% of $t_{SRCOND}(n-1)$ as shown in Figure 53.

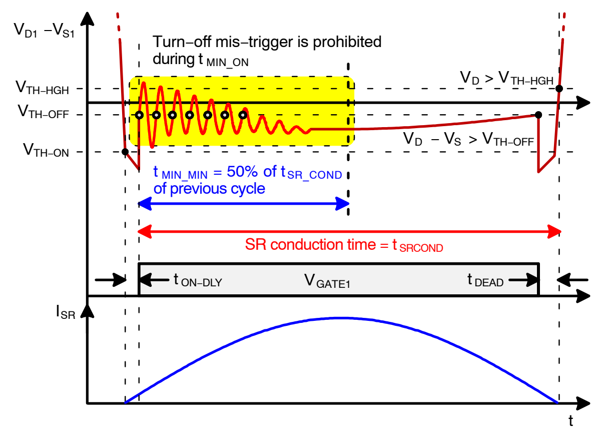


Figure 51. Minimum Turn−on time and Turn−off Mis−triggering

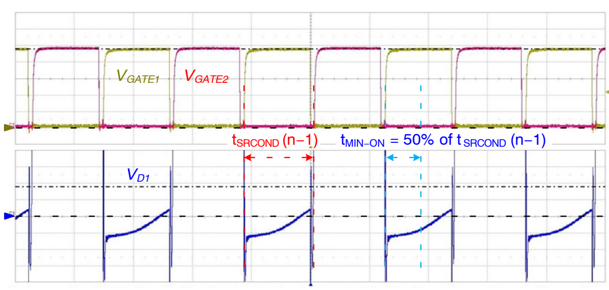


Figure 52. Minimum Turn−on Time t_{MIN-ON} when *DLY_EN=0*

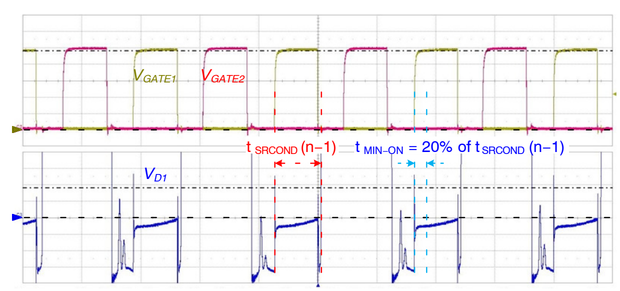


Figure 53. Minimum Turn−on Time t_{MIN-ON} when *DLY_EN=1*

Multi−step V_{TH-OFF}

In heavy−load conditions, V_{TH-OFF} tends to be high. When the switching frequency on the primary side suddenly increases from the heavy−load condition, the SR current conduction duration reduces accordingly. To make the SR controller timely reacts to this transition, we implements a multi−step V_{TH-OFF} function to reduce the effective V_{TH-OFF}, turning off the SR gate earlier, during this transition. Referring to the SR gate on−time of previous switching cycle, before the SR gate on−time reaches 70% ($K_{2ND-TOFF}$) of the previous−cycle on−time, the effective V_{TH-OFF} is temporarily reduces to 60% ($K_{2ND-VOFF}$) of its real value. Thus, the SR gate can be turned off with a lower V_{TH-OFF} during the frequency−increasing transition, providing a safer operation. The multi−step V_{TH-OFF} function is active when *LLD* = 0.

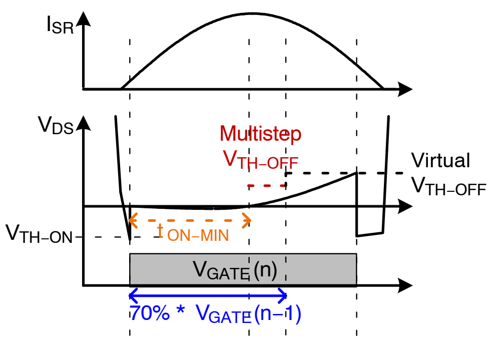


Figure 54. $t_{DEAD} \in [t_{DEAD-LBAND}, t_{DEAD-HBAND}]$

Current Inversion Detection

During SR operation, two types of inversion current may occur. First, in light load condition, capacitive current spike causes leading edge inversion current. In heavy load condition, the body diode of SR MOSFET starts conducting right after the primary side switching transition taking place. However, when the resonance−capacitor voltage amplitude is not large enough in light load condition, the voltage across the magnetizing inductance of the transformer is smaller than the reflected output voltage. Thus, the secondary side SR body diode conduction is delayed until the magnetizing inductor voltage builds up to the reflected output voltage. However, the primary side switching transition can cause capacitive current spike and turn on the body diode of SR MOSFET for a short time as shown in Figure 55, which induces SR turn−on mis−trigger. As a result, the turn−on mis−trigger makes leading edge inversion current in the secondary side.

The second inversion current is trailing edge inversion current caused by excessive SR gate on−time, which is generally due to the minimum on−time t_{MIN-ON}. If t_{MIN-ON} is longer than current transferring duration, trailing edge inversion current can happen as shown in Figure 56. If there is no proper algorithm to prevent this inversion current, severe drain voltage spike can happen due to SR MOSFET hard switching.

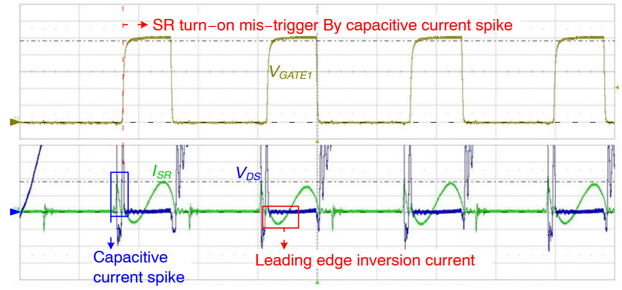


Figure 55. Leading Edge Inversion Current

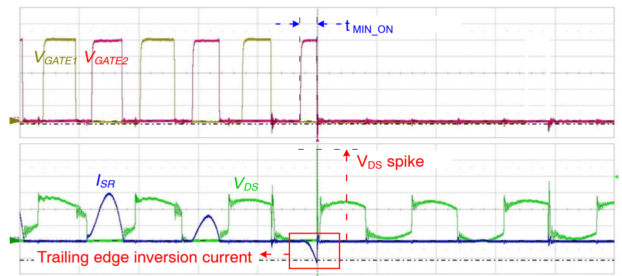


Figure 56. Trailing Edge Inversion Current

To prevent both leading edge and trailing edge inversion currents, NCP4318 has a current inversion detection function *SRCINV*. This function is effective during t_{MIN-ON}. When the SR gate is turned on and the inversion current occurs, the drain sensing voltage of SR MOSFET becomes a positive value. In this condition, if V_{DS} is higher than 0 mV for t_{INV} of the detection confirmation time, *SRCINV* will be triggered and turn off the SR gate immediately. Then, the *DLY_EN* flag goes high and the turn−on delay is increased to $t_{ON-DLY2}$ for the following switching cycles.

When the *LLD* flag is high, V_{TH-OFF} tends to be low, and the V_{TH-OFF} replaces the 0−mV threshold voltage for *SRCINV*. If the gate on−time is longer than t_{MIN-ON}, the virtual V_{TH-OFF} turn−off mechanism will turn off the gate properly.

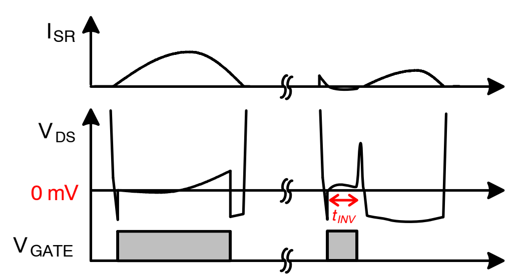


Figure 57. Triggering SRCINV by Leading−edge Inversion Current

Green Mode

In NCP4318, there are two stages to trigger *GREEN* function. *GREEN1* is for low power consumption in light load condition, and *GREEN2* is for preparing a *GREEN1* triggering.

When the LLC controller in the primary side operates in skip mode under light load conditions, making V_{D1} shows no switching waveform for longer than $t_{GRN1-ENT}$, the *GREEN1* mode will be activated as shown in Figure 58. Once NCP4318 is in the *GREEN1* mode, all the major functions are disabled to reduce the operating current down to 100 μA of $I_{DD-GREEN}$. NCP4318 exits from *GREEN1* when four switching cycles are observed from V_{D1} as shown in Figure 59.

Before *GREEN1* being triggered, if the duration of no switching operation is longer than $t_{GRN2-ENT}$, a short *GREEN2* pulse is generated to reset the virtual V_{TH-OFF} and assert *DLY_EN*. *LLD* may also be asserted when V_{TH-OFF} resets to a level lower than η_{LLD1}. Doing so, *GREEN2* prepares new SR operation starting condition and allows soft increment of SR gate pulses for the next switching bundle.

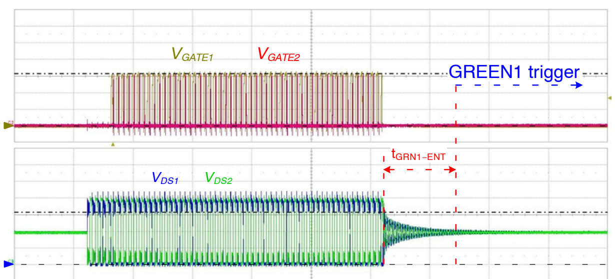


Figure 58. Entering *GREEN1*

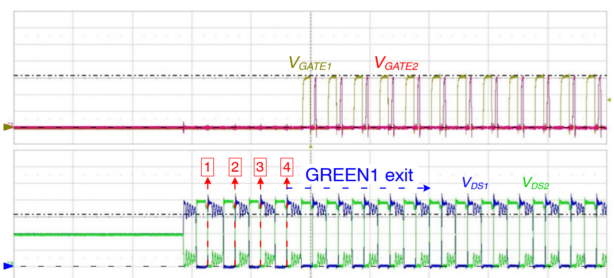


Figure 59. Exit from *GREEN1*

Limitation on SR Gate On−time Increasing Rate

To better cope with transitions of operating frequency, NCP4318 has an optional SR gate on−time increasing−rate limitation function. When this function is enable, the on−time of consecutive SR−gate pulses won't increase too much from their precedent pulse. The increase rate is limited as 550 ns of $t_{GATE-LIM}$ between two consecutive pulses. In other words, when the on−time should change from a smaller value to a larger value, the SR gate takes a few switching cycle to increase its pulse width gradually.

More, when this function is enabled, the maximum pulse width of the SR gate start from 1.2 μs after a *GREEN2* or *SRCINV* event. The maximum pulse width increases up to $t_{SR-MAX-ON}$.

Adaptive V_{GATE} Control

Lowering the gate clamping voltage V_{GATE} reduces gate drive power consumption. Adaptive V_{GATE} control reduces V_{GATE} level when it is a better choice of operation. In NCP4318, there are three condition to trigger the adaptive V_{GATE}. First is the output load condition. In light load condition, to save the SR gate driving current and maximize efficiency, NCP4318 adaptively changes V_{GATE}. As shown in Figure 60, when LLD goes from '0' to '1', the gate clamp voltage reduces from 10 V to 6 V. It could save 40% of gate driving power consumption. In heavy load condition, V_{GATE} resumes to 10 V for lower turn−on resistance R_{DS-ON} of the SR MOSFET, as depicted in Figure 61. There is also a 3−level−V_{GATE} option which set V_{GATE} = 5 V when LLD = 2.

The second condition is the operating frequency. If the LLC operating frequency is higher than 200 kHz of $f_{HFS-EN} = 1/t_{HFS-EN}$ in L−version and 250 kHz in H−version, NCP4318 reduces V_{GATE} for lowering SR gate driving current.

The last condition is junction temperature T_J of the IC. When T_J is higher than 105°C of T_{OTP1}, V_{GATE} reduces to 6 V to reduce heat dissipation of the IC. V_{GATE} resumes to 10 V when T_J is lower than 80°C of $T_{OTP-RST}$.

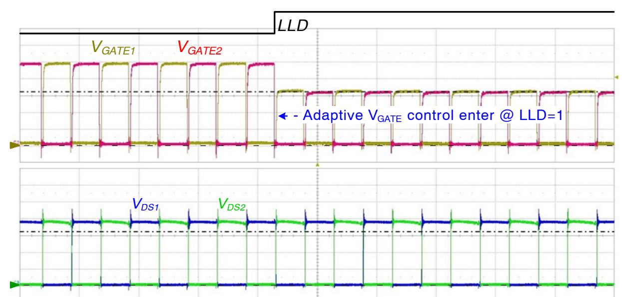


Figure 60. V_{GATE} Reduces when LLD is High

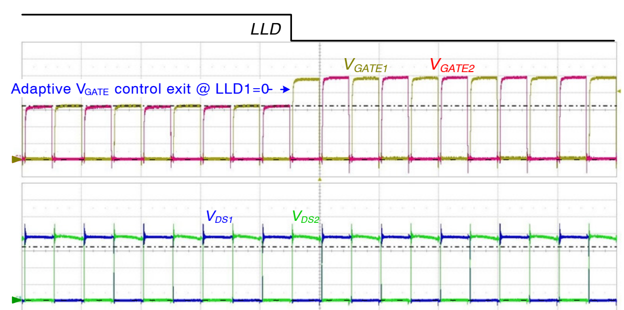


Figure 61. V_{GATE} Resumes When LLD is Low

Soft Start

At the beginning of LLC startup, the operating frequency is severely changed, and the symmetrical duty cycles between the high−side and low−side power switches on the primary side sometimes cannot be guaranteed. To avoid SR operation during the startup transition, NCP4318 implements a soft−start function. After V_{DD} exceeds $V_{DD-GATE-ON}$, the SR gate skips the initial 256 consecutive V_{D1} and V_{D2} switching cycles to check whether LLC system is stable or not. After the first 256 cycles, NCP4318 starts generating SR gate pulses with V_{GATE} = 6 V and $V_{TH-OFF} = V_{TH-OFF-RST}$. If LLD−based adaptive V_{GATE} is enabled, V_{GATE} stays 6 V until *LLD* signal goes to zero. Otherwise, V_{GATE} stays 6 V for another 256 cycles. This allows soft−increment of SR gate pulses and gradual reduction of the SR dead time at startup.

Protections

For higher system reliability, two protections are implemented in NCP4318. First one is the primary shutdown protection. In SR controller point of view, NCP4318 cannot know directly the primary side abnormal gate off, such as by a certain LLC protection or power−off. In that condition, SR gate should be turned off as soon as possible even in minimum on−time. Though *SRCINV* function can turn−off SR gate at that moment, it has a certain delay time t_{INV} for the confirmation. For a faster turning off, a primary shutdown protection is implemented.

When the LLC gate signal in the primary side suddenly cuts down, SR current shows a downward transition, which induces a high *dV*/*dt* on the drain sensing voltage. If the *dV*/*dt* is higher than V_{SD-PRI}/t_{INV}, the primary shutdown protection is triggered and the SR gate turns off immediately. In addition, it asserts *GREEN1*, which makes 4 cycles of SR gate skipping to ignore turn−on mis−trigger caused by energy bouncing in the secondary side. The primary shutdown protection is effective in the leading edge of the SR gate for 70% of its previous−cycle SR gate on−time.

The other protection is the abnormal drain sensing protection. In normal condition, when the SR gate is turn on and higher than 4.5 V, the drain sensing voltage V_D is expected low, which in any case should not exceed V_{TH-HGH}. However, in abnormal condition, due to V_D fluctuation, V_D can be higher than V_{TH-HGH} even when V_{GATE} > 4.5 V. In that condition, NCP4318 triggers the abnormal drain sensing protection, turns off the SR gate and makes *GREEN1* high.

To protect NCP4318 from overheating, NCP4318 stops operation when its junction temperature exceeds T_{OTP2}.

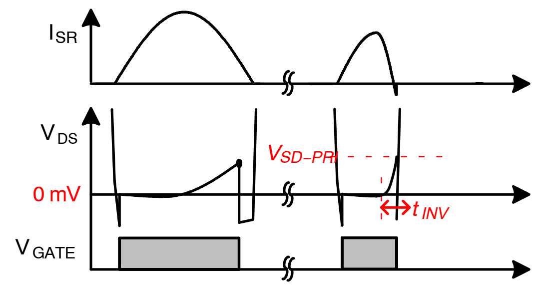


Figure 62. Triggering Primary Shutdown Protection

Recover From $t_{ON-DLY2}$

When the *DLY_EN* flag has been asserted, SR gate turns on after the body diode of the SR MOSFET conducts for $t_{ON-DLY2}$. NCP4318 clears the *DLY_EN* flag by observing the $V_D < V_{TH-ON}$ event. Before the SR gate turning on, if V_D crosses below V_{TH-ON} for only one time, a $\eta_{INV-EXT}$ counter adds by one. This counter resets when the $V_D < V_{TH-ON}$ event happens more than one time in one switching cycle. When the $\eta_{INV-EXT}$ counter has elapsed, the DLY_EN flag is cleared.

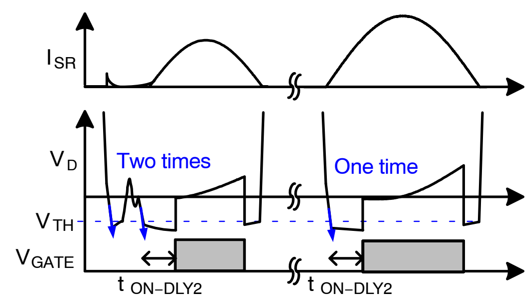


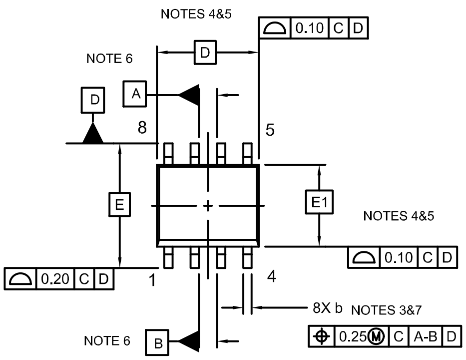
Figure 63. Criterion of Clearing the DLY_EN Flag

PACKAGE DIMENSIONS

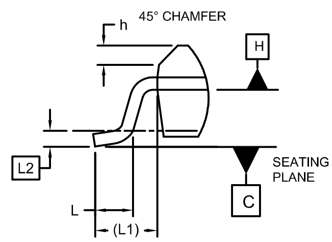
SOIC−8 EP
CASE 751AC
ISSUE D

NOTES:

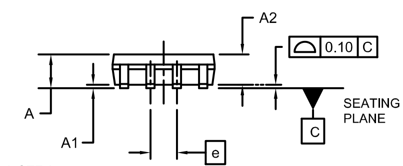
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



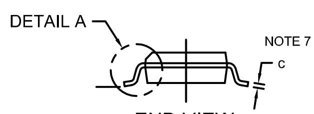
TOP VIEW



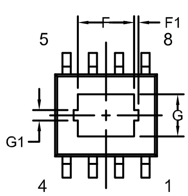
DETAIL A



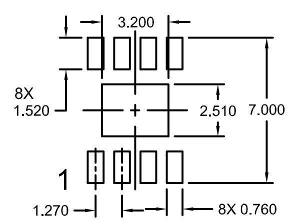
SIDE VIEW



END VIEW



BOTTOM VIEW



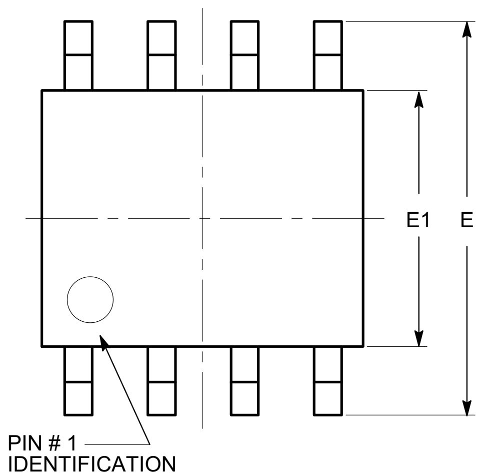
RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D		4.90 BSC	
E		6.00 BSC	
E1		3.90 BSC	
e		1.27 BSC	
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1		1.04 REF	
L2		0.25 REF	
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

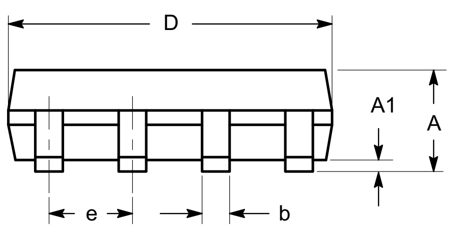
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

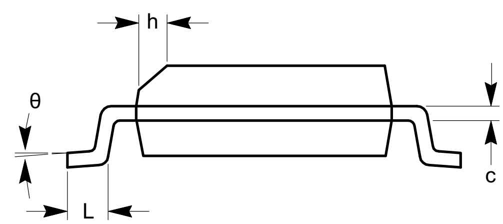


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative