TPS76901-Q1, TPS76912-Q1, TPS76915-Q1
TPS76918-Q1, TPS76925-Q1, TPS76927-Q1
TPS76928-Q1, TPS76930-Q1, TPS76933-Q1, TPS76950-Q1

SGLS118D – DECEMBER 2001 – REVISED SEPTEMBER 2016

TPS769xx-Q1 Ultralow-Power 100-mA Low-Dropout Linear Regulators

1 Features

- Qualified for Automotive Applications
- 100-mA Low-Dropout Regulator
- Available in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V and 5-V Fixed-Output and Adjustable Versions
- Only 17-µA Quiescent Current at 100 mA
- 1-µA Quiescent Current in Standby Mode
- Dropout Voltage Typically 71 mV at 100 mA
- Overcurrent Limitation
- —40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package

2 Applications

- ADAS Modules
- RF Modules
- Wireless Modules
- General Noise-Sensitive Applications

3 Description

The TPS769xx-Q1 family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, ultralow-power operation, and miniaturized packaging. These regulators feature low-dropout voltages and ultralow quiescent current compared to conventional LDO regulators. Offered in a 5-pin small outline integrated-circuit SOT-23 package, the TPS769xx-Q1 series of devices are ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 71 mV at 100 mA of load current (TPS76950-Q1), and is directly proportional to the load current. Because the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (28 µA maximum) and is stable over the entire range of output load current (0 mA to 100 mA). The ultralow-dropout voltage feature and ultralow-power operation result in a significant increase in system battery operating life, making this device suitable for use in automotive applications.

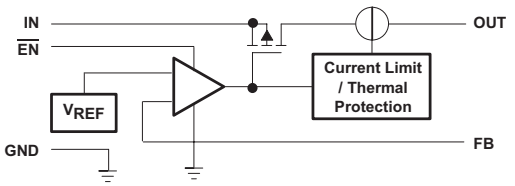
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS769xx-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

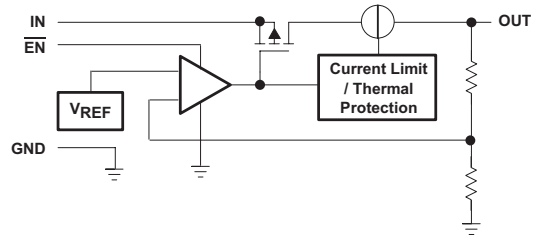
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagrams

TPS76901-Q1



TPS769xx-Q1



TPS76933-Q1 Ground Current vs Free-Air Temperature

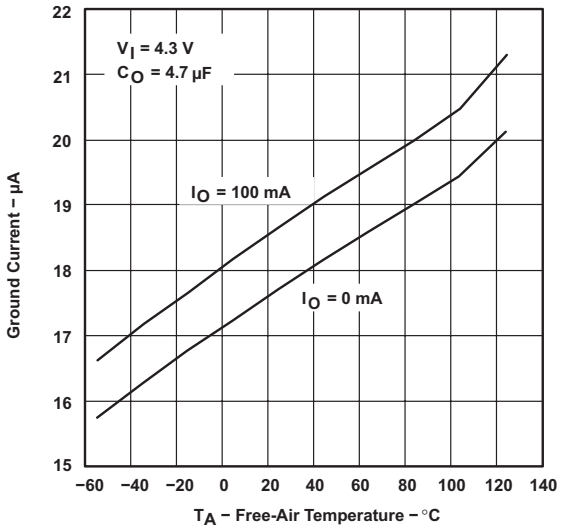


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2012) to Revision D **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Ordering Information* table, see POA at the end of the data sheet ... 1

Changes from Revision B (April 2008) to Revision C **Page**

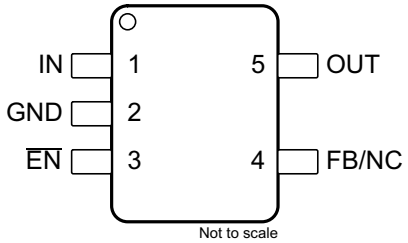
- Changed TPS769xx part names to TPS769xx-Q1 in text and images. ... 3
- Updated Figures 17 and 19 to include region of Instability below 0.2 Ω. ... 9

5 Description (continued)

The TPS769xx-Q1 devices also feature a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 µA (typical) at T_J = 25°C. The TPS769xx-Q1 devices are offered in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.2 V to 5.5 V).

6 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Input supply voltage
2	GND	—	Ground
3	$\overline{EN}$	I	Enable input
4	FB/NC	I	Feedback voltage (TPS76901-Q1 only) No connection (Fixed options only)
5	OUT	O	Regulated output voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Input voltage(2)	–0.3	13.5	V
	Voltage range at $\overline{EN}$	–0.3	V_I + 0.3	V
	Voltage on OUT, FB		7	V
	Peak output current	Internally Limited		
	Continuous total power dissipation	See *Dissipation Ratings*		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±YYY	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage (1)	2.7	10	V
V_O	Output voltage	1.2	5.5	V
I_O	Continuous output current (2)	0	100	mA
T_J	Operating junction temperature	—40	125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula: $V_I(min) = V_O(max) + V_{DO}(max\ load)$
(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

7.4 Thermal Information

THERMAL METRIC (1)		TPS769xx-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	117.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating free-air temperature range, $V_I = V_O$ (typ) + 1 V, I_O = 100 mA, $\overline{EN}$ = 0 V, C_o = 4.7 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 ∝A to 100 mA load) (1)	TPS76901-Q1	1.2 V ≤ V_O ≤ 5.5 V, T_J = 25°C		V_O		V
		1.2 V ≤ V_O ≤ 5.5 V, T_J = –40°C to 125°C	0.97 V_O		1.03 V_O	
	TPS76912-Q1	T_J = 25°C, 2.7 V < V_{IN} < 10 V		1.224		
		T_J = –40°C to 125°C, 2.7 V < V_{IN} < 10 V	1.187		1.261	
	TPS76915-Q1	T_J = 25°C, 2.7 V < V_{IN} < 10 V		1.5		
		T_J = –40°C to 125°C, 2.7 V < V_{IN} < 10 V	1.455		1.545	
	TPS76918-Q1	T_J = 25°C, 2.8 V < V_{IN} < 10 V		1.8		
		T_J = –40°C to 125°C, 2.8 V < V_{IN} < 10 V	1.746		1.854	
	TPS76925-Q1	T_J = 25°C, 3.5 V < V_{IN} < 10 V		2.5		
		T_J = –40°C to 125°C, 3.5 V < V_{IN} < 10 V	2.425		2.575	
	TPS76927-Q1	T_J = 25°C, 3.7 V < V_{IN} < 10 V		2.7		
		T_J = –40°C to 125°C, 3.7 V < V_{IN} < 10 V	2.619		2.781	
	TPS76928-Q1	T_J = 25°C, 3.8 V < V_{IN} < 10 V		2.8		
		T_J = –40°C to 125°C, 3.8 V < V_{IN} < 10 V	2.716		2.884	
	TPS76930-Q1	T_J = 25°C, 4 V < V_{IN} < 10 V		3		
		T_J = –40°C to 125°C, 4 V < V_{IN} < 10 V	2.91		3.09	
	TPS76933-Q1	T_J = 25°C, 4.3 V < V_{IN} < 10 V		3.3		
		T_J = –40°C to 125°C, 4.3 V < V_{IN} < 10 V	3.201		3.399	
	TPS76950-Q1	T_J = 25°C, 6 V < V_{IN} < 10 V		5		
		T_J = —40°C to 125°C, 6 V < V_{IN} < 10 V	4.85		5.15	

(1) Minimum IN operating voltage is 2.7 V or V_O (typ) + 1 V, whichever is greater. The maximum IN voltage is 10 V, minimum output current is 10 µA, and maximum output current is 100 mA.

Electrical Characteristics (continued)

over recommended operating free-air temperature range, $V_I = V_O$ (typ) + 1 V, I_O = 100 mA, $\overline{EN}$ = 0 V, C_o = 4.7 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent current (GND current)(1)(2)		$\overline{EN}$ = 0 V, 0 mA < I_O < 100 mA, T_J = 25°C		17		µA
		$\overline{EN}$ = 0 V, I_O = 100 mA, T_J = –40°C to 125°C			28	
Load regulation		$\overline{EN}$ = 0 V, I_O = 0 to 100 mA, T_J = 25°C		12		mV
Output voltage line regulation ($\Delta V_O/V_O$) (2)		V_O + 1 V < V_I ≤ 10 V, T_J = 25°C(1)		0.04		%/V
		V_O + 1 V < V_I ≤ 10 V, T_J = –40°C to 125°C(1)			0.1	
Output noise voltage		BW = 300 Hz to 50 kHz, C_o = 10 ∝F, T_J = 25°C		190		μV_{rms}
Output current limit		V_O = 0 V(1)		350	750	mA
Standby current		$\overline{EN}$ = V_I, 2.7 < V_I < 10 V		1		µA
		T_J = —40°C to 125°C			2	
FB input current		FB = 1.224 V (TPS76901-Q1)	–1		1	µA
High level enable input voltage		2.7 V < V_I < 10 V	1.7			V
Low level enable input voltage		2.7 V < V_I < 10 V			0.9	V
Power supply ripple rejection		f = 1 kHz, C_o = 10 ∝F, T_J = 25°C		60		dB
Input current ($\overline{EN}$)		$\overline{EN}$ = 0 V	–1	0	1	µA
		$\overline{EN}$ = V_I	–1		1	
Dropout voltage(3)	TPS76928-Q1	I_O = 50 mA, T_J = 25°C		60		mV
		I_O = 50 mA, T_J = –40°C to 125°C			125	
		I_O = 100 mA, T_J = 25°C		122		
		I_O = 100 mA, T_J = –40°C to 125°C			245	
	TPS76930-Q1	I_O = 50 mA, T_J = 25°C		57		
		I_O = 50 mA, T_J = –40°C to 125°C			115	
		I_O = 100 mA, T_J = 25°C		115		
		I_O = 100 mA, T_J = –40°C to 125°C			230	
	TPS76933-Q1	I_O = 50 mA, T_J = 25°C		48		
		I_O = 50 mA, T_J = –40°C to 125°C			100	
		I_O = 100 mA, T_J = 25°C		98		
		I_O = 100 mA, T_J = –40°C to 125°C			200	
	TPS76950-Q1	I_O = 50 mA, T_J = 25°C		35		
		I_O = 50 mA, T_J = –40°C to 125°C			85	
		I_O = 100 mA, T_J = 25°C		71		
		I_O = 100 mA, T_J = –40°C to 125°C			170	

(2) If V_O ≤ 1.8 V then V_{Imin} = 2.7 V, V_{Imax} = 10 V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{Imax} - 2.7\ V)}{100} \times 1000$$

If V_O ≥ 2.5 V then $V_{Imin} = V_O$ + 1 V, V_{Imax} = 10 V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{Imax} - (V_O + 1V))}{100} \times 1000$$

(3) The IN voltage equals V_O (typ) — 100 mV; the TPS76901-Q1 output voltage is set to 3.3 V nominal with an external resistor divider. TPS76912-Q1, TPS76915-Q1, TPS76918-Q1, TPS76925-Q1, and TPS76927-Q1 dropout voltage is limited by input voltage range limitations.

7.6 Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K(1)	DBV	65.8°C/W	259°C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K(2)	DBV	65.8°C/W	180°C/W	5.6 mW/°C	555 mW	305 mW	222 mW

(1) The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

7.7 Typical Characteristics

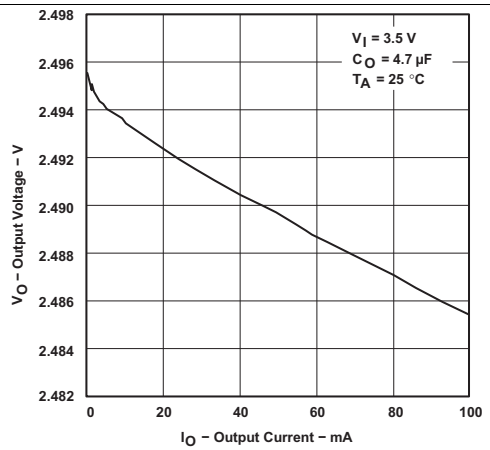


Figure 1. TPS76925-Q1 Output Voltage vs Output Current

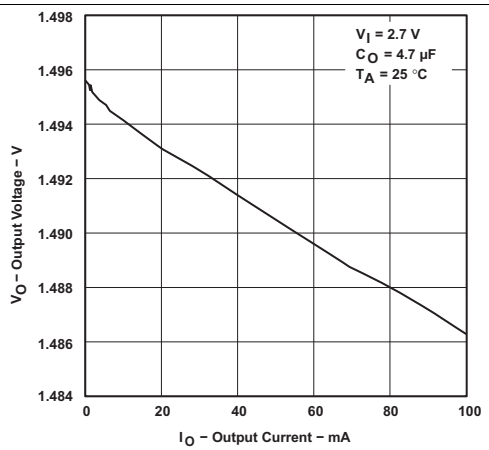


Figure 2. TPS76915-Q1 Output Voltage vs Output Current

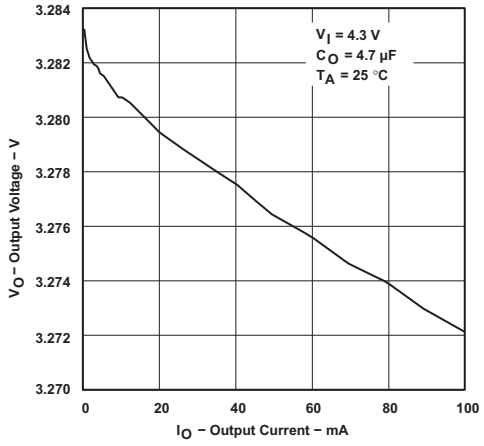


Figure 3. TPS76933-Q1 Output Voltage vs Output Current

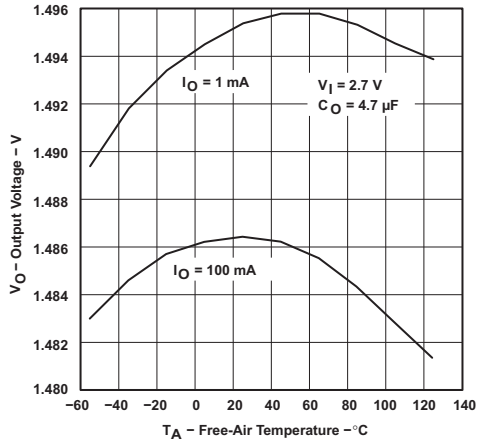


Figure 4. TPS76915-Q1 Output Voltage vs Free-Air Temperature

Typical Characteristics (continued)

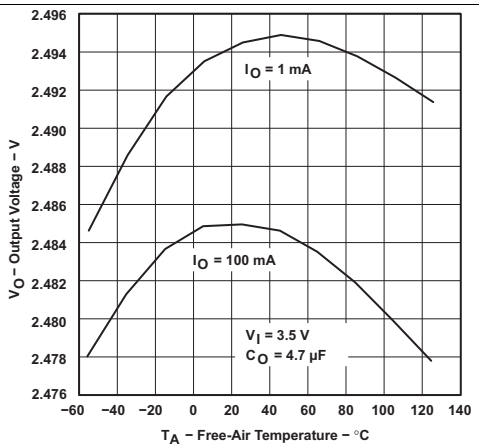


Figure 5. TPS76925-Q1 Output Voltage vs Free-Air Temperature

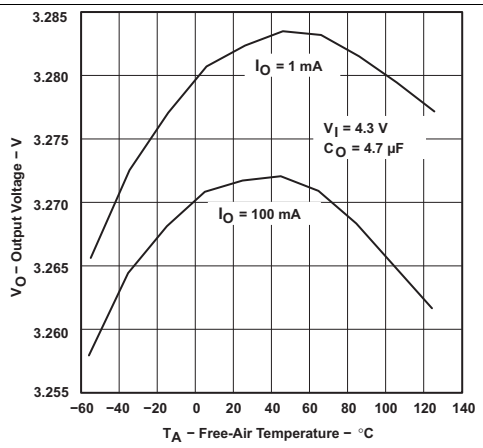


Figure 6. TPS76933-Q1 Output Voltage vs Free-Air Temperature

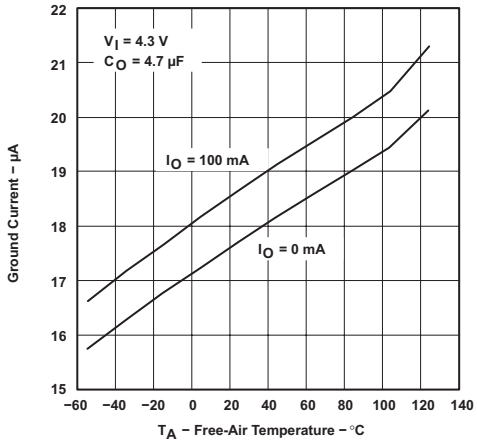


Figure 7. TPS76933-Q1 Ground Current vs Free-Air Temperature

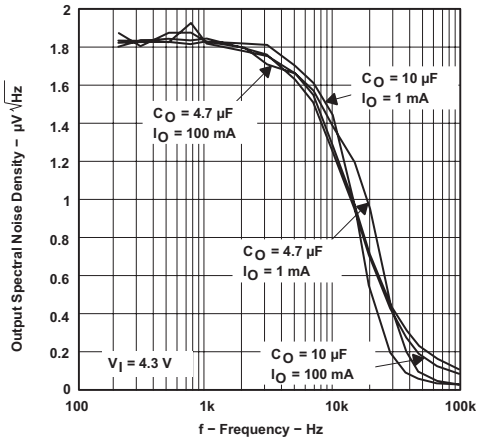


Figure 8. TPS76933-Q1 Output Spectral Noise Density vs Frequency

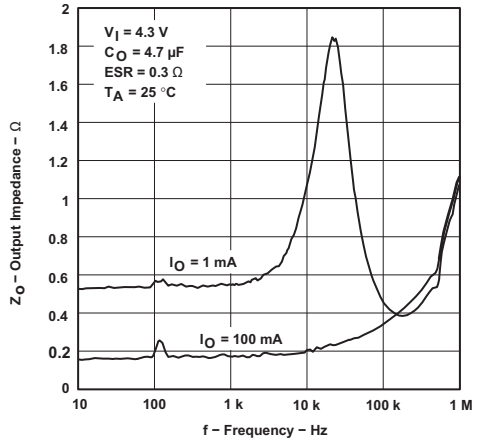


Figure 9. Output Impedance vs Frequency

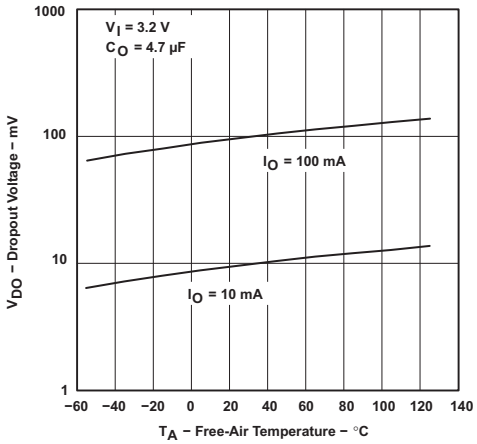


Figure 10. TPS76933-Q1 Dropout Voltage vs Free-Air Temperature

Typical Characteristics (continued)

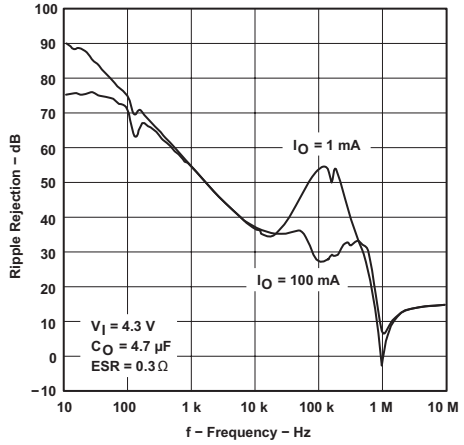


Figure 11. TPS76933-Q1 Ripple Rejection vs Frequency

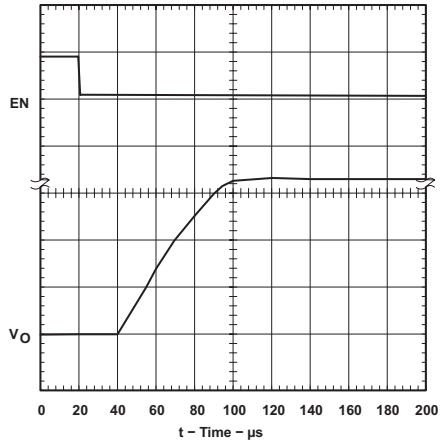


Figure 12. LDO Start-Up Time

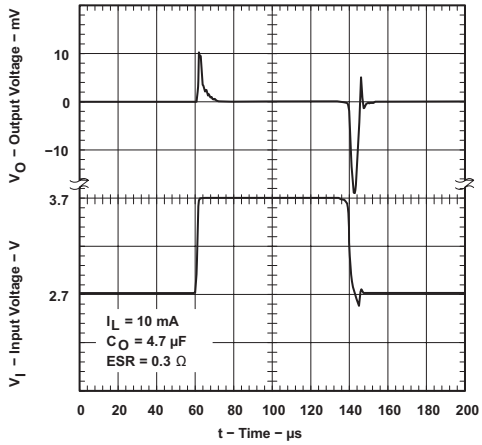


Figure 13. TPS76915-Q1 Line Transient Response

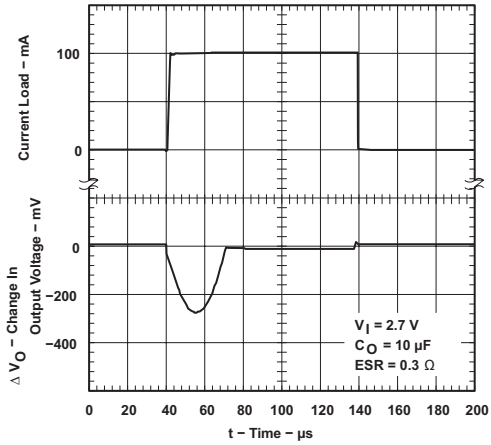


Figure 14. TPS76915-Q1 Load Transient Response

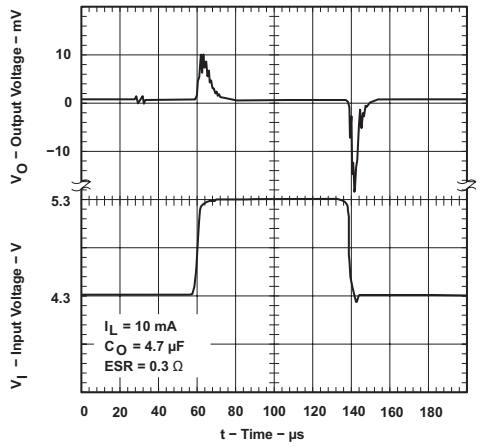


Figure 15. TPS76933-Q1 Line Transient Response

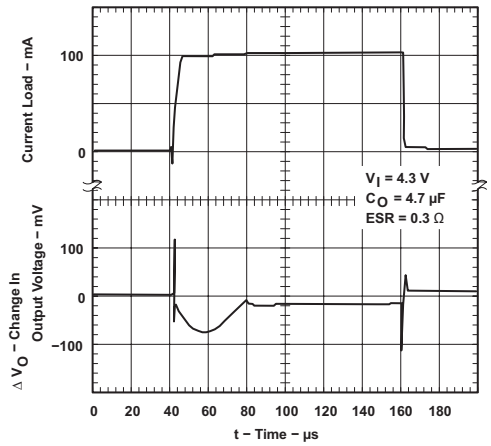


Figure 16. TPS76933-Q1 Load Transient Response

Typical Characteristics (continued)

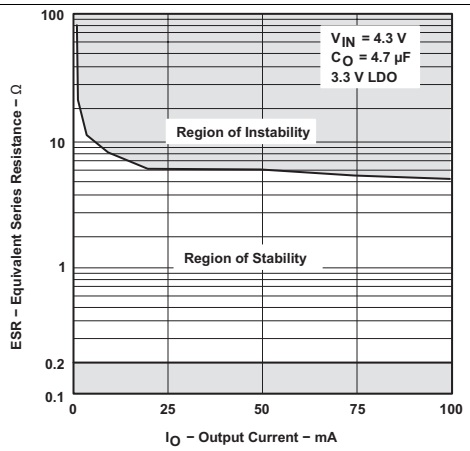


Figure 17. TPS76933-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

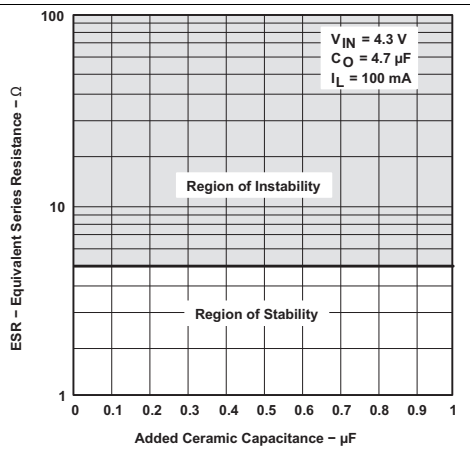


Figure 18. TPS76933-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Added Ceramic Capacitance

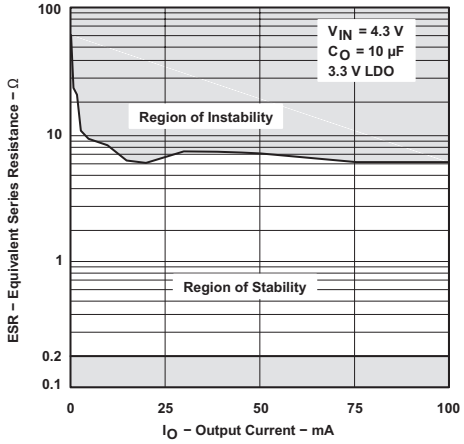


Figure 19. TPS76933-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

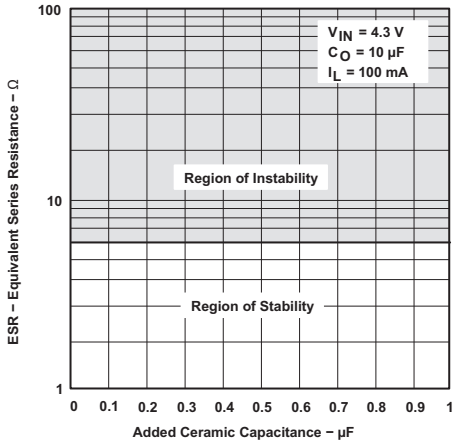


Figure 20. TPS76933-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Added Ceramic Capacitance

8 Detailed Description

8.1 Overview

The TPS769xx-Q1 family of low-dropout (LDO) regulators are optimized for use in battery-operated equipment and automotive applications. They feature extremely low dropout voltages, low quiescent current (17 µA nominally), and enable inputs to reduce supply currents to 1 µA when the regulators are turned off.

8.2 Functional Block Diagrams

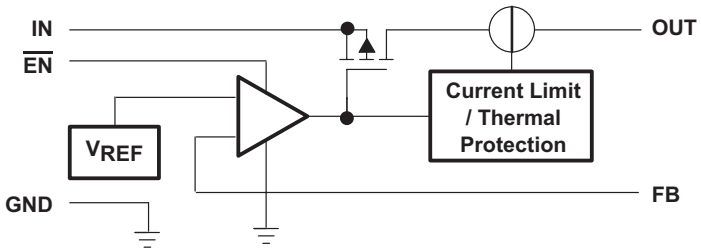


Figure 21. TPS76901-Q1 Functional Block Diagram

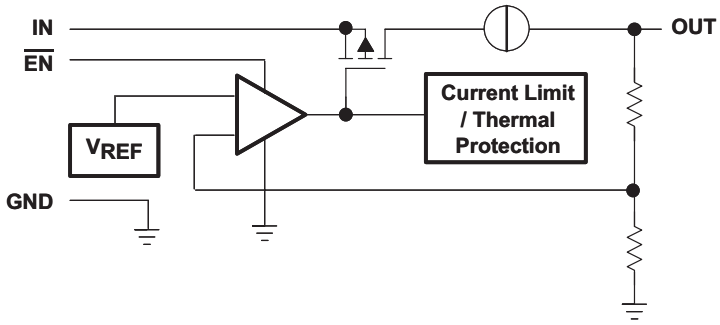


Figure 22. TPS769xx-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 Regulator Protection

The TPS769xx-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS769xx-Q1 features internal current limiting and thermal protection. During normal operation, the TPS769xx-Q1 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

8.4 Device Functional Modes

At 100-mA loads the device operates in low power mode and the quiescent current consumption is reduced to 28 µA (maximum).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

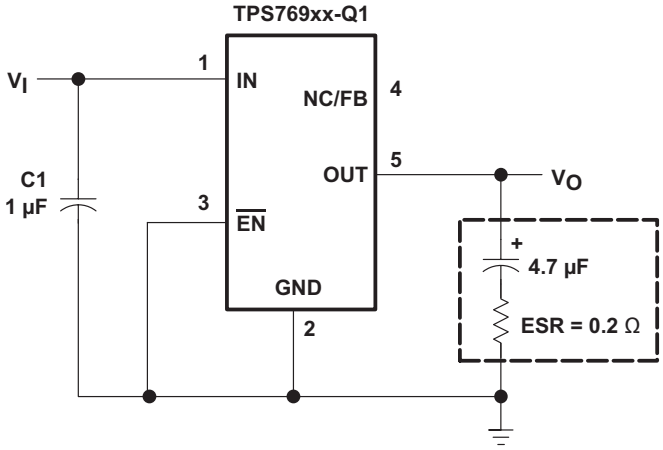
9.1 Application Information

The TPS769xx-Q1 uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS769xx-Q1 is essentially constant from no load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the $\overline{EN}$ input disables the TPS769xx-Q1 internal circuitry, reducing the supply current to 1 µA. A voltage of less than 0.9 V on the $\overline{EN}$ input enables the TPS769xx and enables normal operation to resume. The $\overline{EN}$ input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

9.2 Typical Application



TPS76912-Q1, TPS76915-Q1, TPS76918-Q1, TPS76925-Q1, TPS76927-Q1, TPS76928-Q1, TPS76930-Q1, TPS76933-Q1, TPS76950-Q1 (fixed-voltage options).

Figure 23. Typical Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 10 V
Output voltage	2.5 V to 5 V
Output current rating	100 mA
Output capacitor	4.7 µF to 10 µF
Output capacitor ESD range	200 mΩ to 10 Ω

9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitor Requirements

Although not required, TI recommends a 0.047-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS769xx-Q1, to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS769xx-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 µF. The ESR (equivalent series resistance) of the capacitor must be between 0.2 Ω and 10 Ω. to ensure stability. Capacitor values larger than 4.7 µF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 µF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7-µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may therefore require the addition of a low value series resistor to ensure stability.

Table 2. Capacitor Selection

PART NO.	MFR.	VALUE	MAX ESR	SIZE (H × L × W)(1)
T494B475K016AS	KEMET	4.7 µF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 µF	1.5 Ω	1.3 × 7 × 2.7
695D106x003562T	SPRAGUE	10 µF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 × 6 × 3.2

(1) Size is in mm. ESR is maximum resistance in Ω at 100 kHz and T_A = 25°C. Contact manufacturer for minimum ESR values.

9.2.2.2 Output Voltage Programming

The output voltage of the TPS76901-Q1 adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using Equation 1.

$$V_O = V_{ref} \times (1 + \frac{R1}{R2})$$

where

- The internal reference voltage (V_{REF}) = 1.224 V (typical) (1)

Resistors R1 and R2 must be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values must be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using Equation 2.

$$R1 = (\frac{V_O}{V_{ref}} - 1) \times R2 \quad (2)$$

Table 3. Output Voltage Programming Guide

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)(1)	
	R1	R2
2.5	174	169
3.3	287	169
3.6	324	169
4	383	169
5	523	169

(1) 1% values shown.

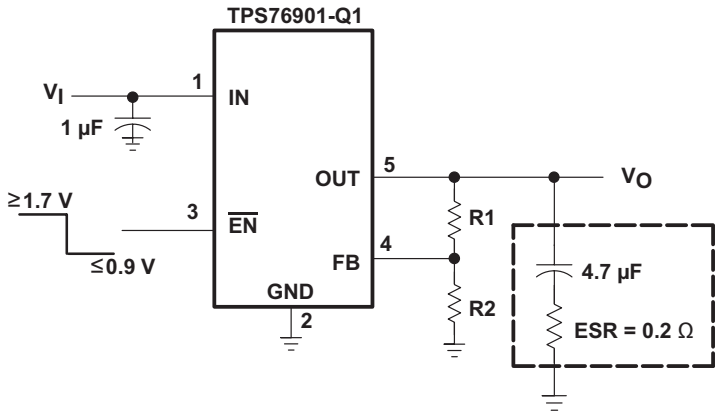


Figure 24. TPS76901-Q1 Adjustable LDO Regulator Programming

9.2.3 Application Curves

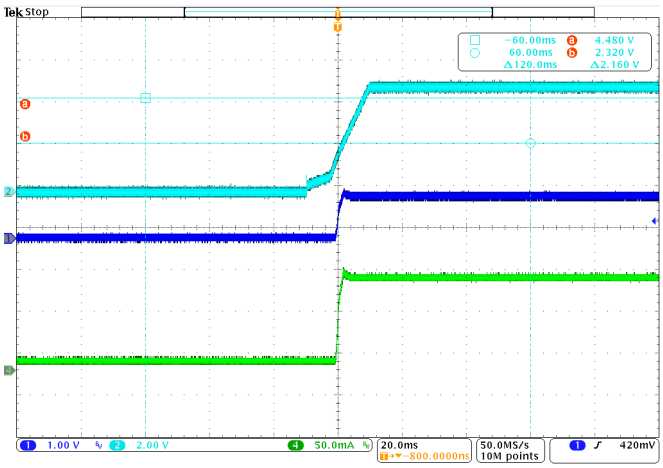


Figure 25. Power-Up Waveform (CH1 VOUT, CH2 VIN, CH4 IOUT)

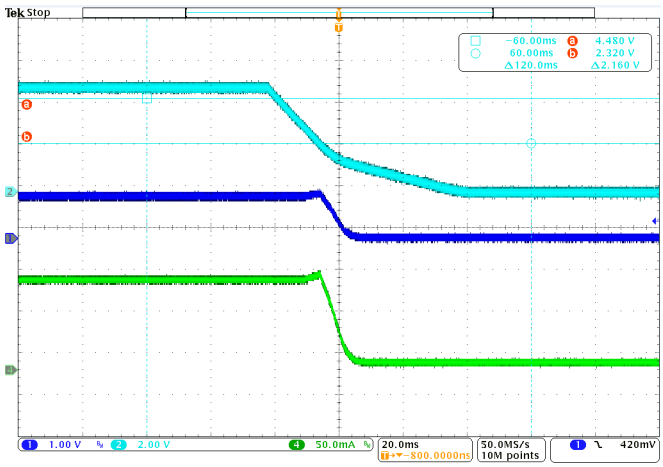


Figure 26. Power-Down Waveform (CH1 VOUT, CH2 VIN, CH4 IOUT)

10 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 2.7 V and 10 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, TI recommends adding an electrolytic capacitor with a value of 1 µF and a ceramic bypass capacitor at the input.

11 Layout

11.1 Layout Guidelines

For the LDO power supply, especially these high voltage and large current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, it is recommended to spread the GND as large as possible and put enough thermal vias on the thermal pad. Figure 27 shows an example layout.

11.2 Layout Example

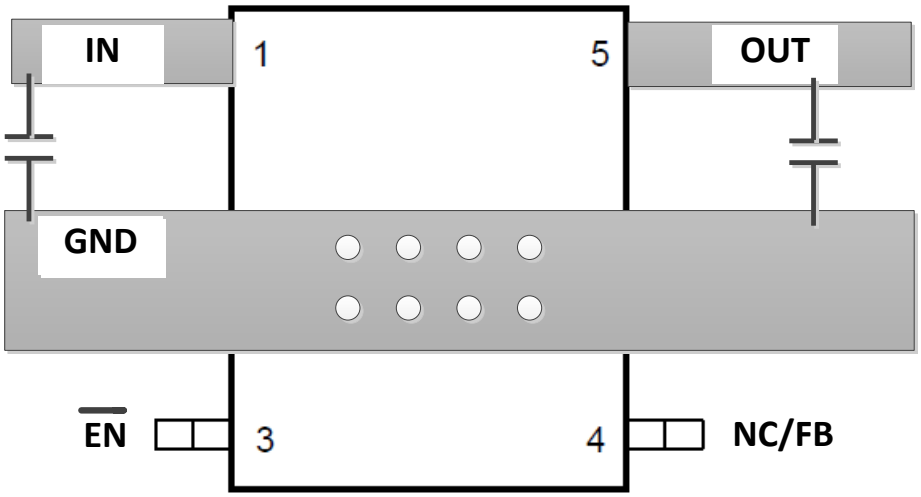


Figure 27. Layout Recommendation

11.3 Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature must be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 3.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (3)$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.
- T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 4.

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS76901-Q1	Click here	Click here	Click here	Click here	Click here
TPS76912-Q1	Click here	Click here	Click here	Click here	Click here
TPS76915-Q1	Click here	Click here	Click here	Click here	Click here
TPS76918-Q1	Click here	Click here	Click here	Click here	Click here
TPS76925-Q1	Click here	Click here	Click here	Click here	Click here
TPS76927-Q1	Click here	Click here	Click here	Click here	Click here
TPS76928-Q1	Click here	Click here	Click here	Click here	Click here
TPS76930-Q1	Click here	Click here	Click here	Click here	Click here
TPS76933-Q1	Click here	Click here	Click here	Click here	Click here
TPS76950-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me*to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76901QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCFQ	Samples
TPS76901QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCFQ	Samples
TPS76915QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCHQ	Samples
TPS76918QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCIQ	Samples
TPS76918QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCIQ	Samples
TPS76925QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCJQ	Samples
TPS76925QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCJQ	Samples
TPS76927QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCKQ	Samples
TPS76928QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCLQ	Samples
TPS76930QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCMQ	Samples
TPS76930QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCMQ	Samples
TPS76933QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCNQ	Samples
TPS76933QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCNQ	Samples
TPS76950QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCOQ	Samples
TPS76950QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCOQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS769-Q1 :

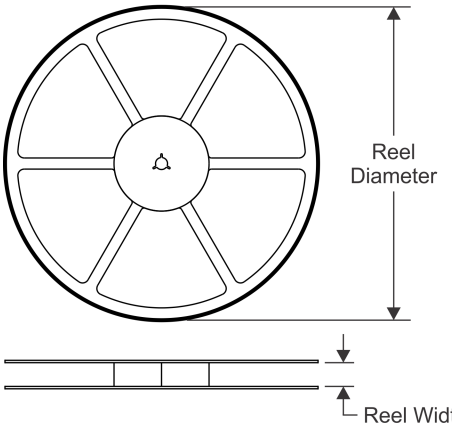
- Catalog : TPS769

NOTE: Qualified Version Definitions:

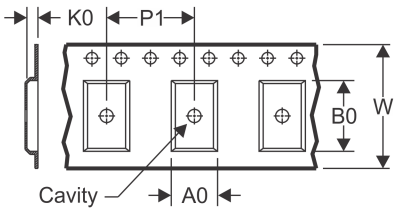
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

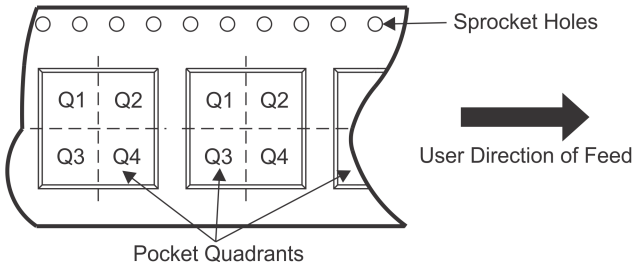


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

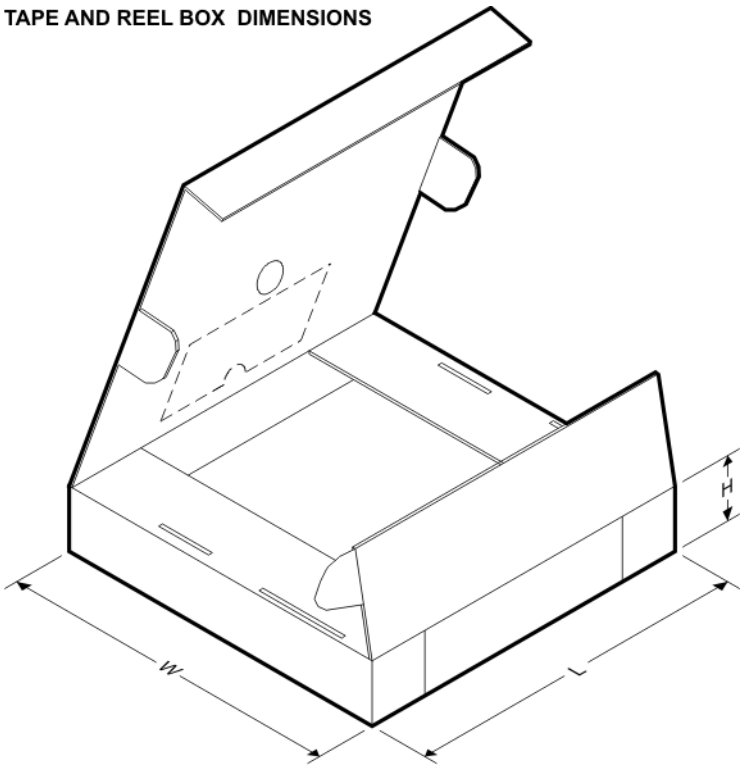
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76901QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76901QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76915QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76918QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76918QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76925QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76925QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76927QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76928QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76930QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76930QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76933QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76933QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76950QDBVRG4Q1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS76950QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

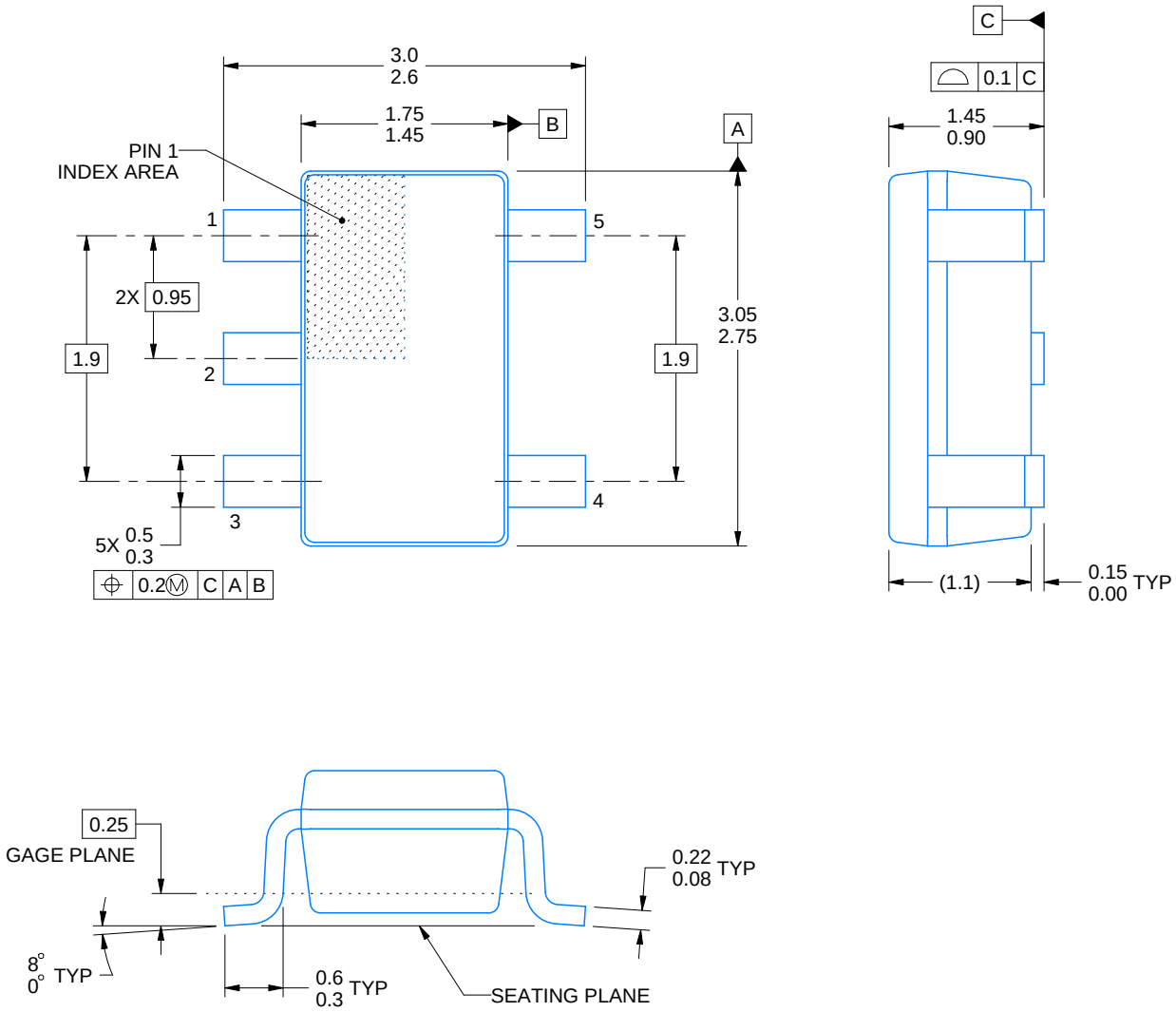
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76901QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76901QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76915QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76918QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76918QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76925QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76925QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76927QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76928QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76930QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76930QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76933QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76933QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76950QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76950QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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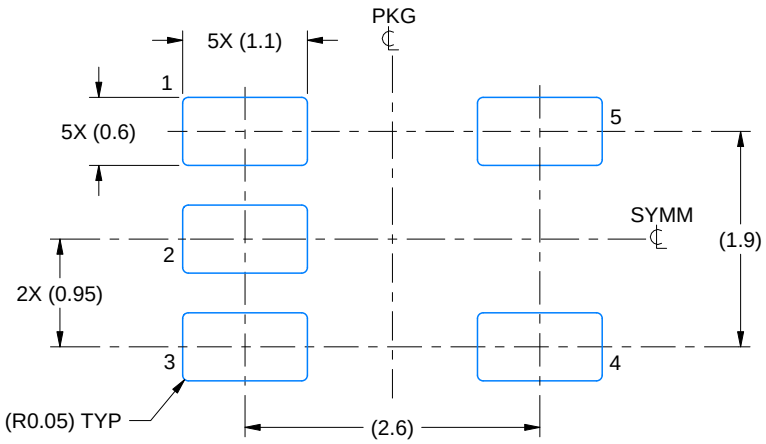
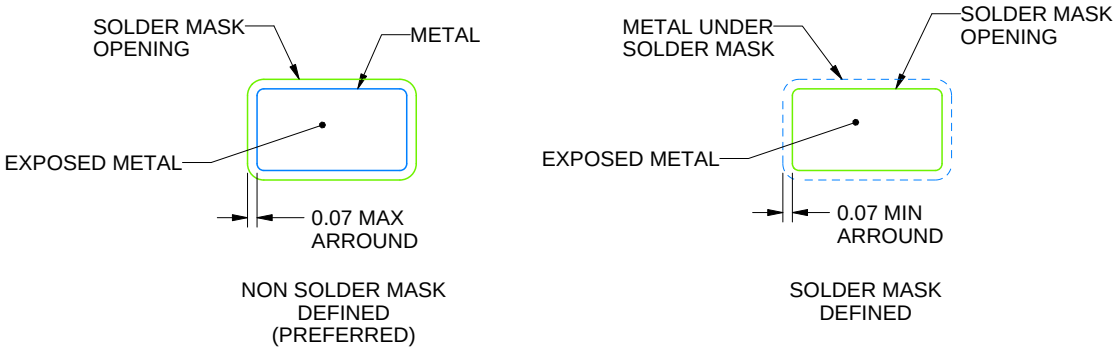
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

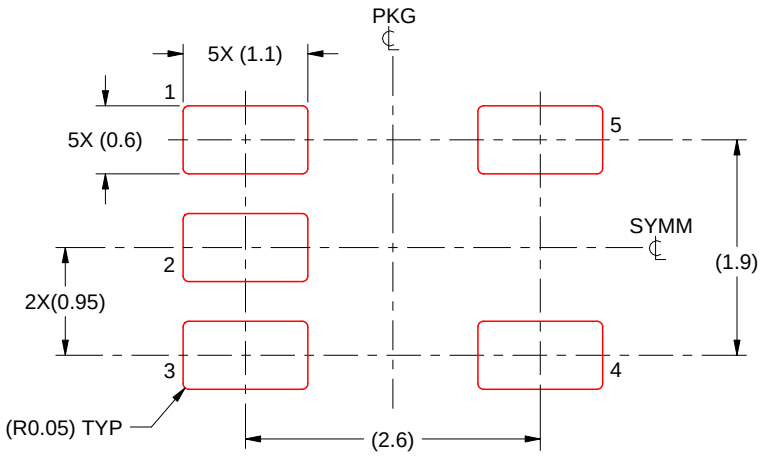


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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