

NTMFD4901NF

MOSFET – Power, Dual, N-Channel with Integrated Schottky, SO8FL

30 V, High Side 18 A / Low Side 30 A

Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Low Side MOSFET with Integrated Schottky
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

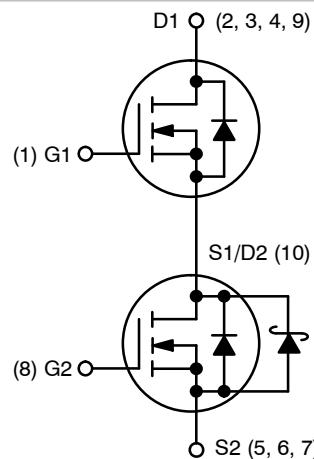
- DC-DC Converters
- System Voltage Rails
- Point of Load



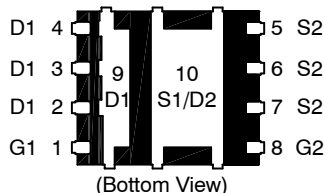
ON Semiconductor®

<http://onsemi.com>

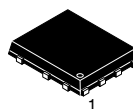
| V _{(BR)DSS} | R _{DS(ON)} MAX | I _D MAX |
|-----------------------|-------------------------|--------------------|
| Q1 Top FET 30 V | 6.5 mΩ @ 10 V | 18 A |
| | 10 mΩ @ 4.5 V | |
| Q2 Bottom FET 30 V | 2.35 mΩ @ 10 V | 30 A |
| | 3.5 mΩ @ 4.5 V | |



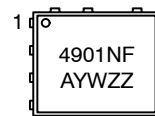
PIN CONNECTIONS



MARKING DIAGRAM



DFN8
CASE 506BX



4901NF = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTMFD4901NF

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|--|----------------|-------------|------------------|------------------|
| Drain-to-Source Voltage | Q1 | V_{DSS} | 30 | V | |
| Drain-to-Source Voltage | Q2 | | | | |
| Gate-to-Source Voltage | Q1 | V_{GS} | ± 20 | V | |
| Gate-to-Source Voltage | Q2 | | | | |
| Continuous Drain Current $R_{\theta JA}$ (Note 1) | $T_A = 25^\circ\text{C}$ | Q1 | 13.5 | A | |
| | | Q2 | 23.4 | | |
| | $T_A = 85^\circ\text{C}$ | Q1 | 9.7 | | |
| | | Q2 | 16.9 | | |
| Power Dissipation $R_{\theta JA}$ (Note 1) | $T_A = 25^\circ\text{C}$ | Q1 | 1.90 | W | |
| | | Q2 | 2.07 | | |
| Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1) | $T_A = 25^\circ\text{C}$ | Q1 | 18.2 | A | |
| | | Q2 | 30.3 | | |
| | $T_A = 85^\circ\text{C}$ | Q1 | 13.1 | | |
| | | Q2 | 21.8 | | |
| Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1) | $T_A = 25^\circ\text{C}$ | Q1 | 3.45 | W | |
| | | Q2 | 3.45 | | |
| Continuous Drain Current $R_{\theta JA}$ (Note 2) | $T_A = 25^\circ\text{C}$ | Q1 | 10.3 | A | |
| | | Q2 | 17.9 | | |
| | $T_A = 85^\circ\text{C}$ | Q1 | 7.4 | | |
| | | Q2 | 12.9 | | |
| Power Dissipation $R_{\theta JA}$ (Note 2) | $T_A = 25^\circ\text{C}$ | Q1 | 1.10 | W | |
| | | Q2 | 1.20 | | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}$ $t_p = 10 \mu\text{s}$ | Q1 | 60 | A | |
| | | Q2 | 100 | | |
| Operating Junction and Storage Temperature | Q1 | T_J, T_{STG} | -55 to +150 | $^\circ\text{C}$ | |
| | Q2 | | | | |
| Source Current (Body Diode) | Q1 | I_S | 3.4 | A | |
| | Q2 | | 4.9 | | |
| Drain to Source dV/dt | | dV/dt | 6 | V/ns | |
| Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = XX$ A _{pk} , $L = 0.1$ mH, $R_G = 25 \Omega$) | 24 A | Q1 | EAS | 28.8 | mJ |
| | 48 A | Q2 | EAS | 115 | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

NTMFD4901NF

THEMAL RESISTANCE MAXIMUM RATINGS

| Parameter | FET | Symbol | Value | Unit |
|---|-----|-----------------|-------|------|
| Junction-to-Ambient – Steady State (Note 3) | Q1 | $R_{\theta JA}$ | 65.9 | °C/W |
| | Q2 | | 60.5 | |
| Junction-to-Ambient – Steady State (Note 4) | Q1 | $R_{\theta JA}$ | 113.2 | |
| | Q2 | | 104 | |
| Junction-to-Ambient – ($t \leq 10$ s) (Note 3) | Q1 | $R_{\theta JA}$ | 36.2 | |
| | Q2 | | 36.2 | |

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | FET | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----|---------------------|-------------------------------------|---------------------------|-----|-----------|---------|
| OFF CHARACTERISTICS | | | | | | | |
| Drain-to-Source Break-down Voltage | Q1 | $V_{(BR)DSS}$ | $V_{GS} = 0$ V, $I_D = 250$ μ A | 30 | | | V |
| | Q2 | | $V_{GS} = 0$ V, $I_D = 1$ mA | 30 | | | |
| Drain-to-Source Break-down Voltage Temperature Coefficient | Q1 | $V_{(BR)DSS} / T_J$ | | | 18 | | mV / °C |
| | Q2 | | | | 15 | | |
| Zero Gate Voltage Drain Current | Q1 | I_{DSS} | $V_{GS} = 0$ V, $V_{DS} = 24$ V | $T_J = 25^\circ\text{C}$ | | 1 | μ A |
| | | | | $T_J = 125^\circ\text{C}$ | | 10 | |
| | Q2 | | $V_{GS} = 0$ V, $V_{DS} = 24$ V | $T_J = 25^\circ\text{C}$ | | 500 | |
| | | | | | | | |
| Gate-to-Source Leakage Current | Q1 | I_{GSS} | $V_{GS} = 0$ V, $V_{DS} = \pm 20$ V | | | ± 100 | nA |
| | Q2 | | | | | ± 100 | |

ON CHARACTERISTICS (Note 5)

| | | | | | | | | |
|--|----|--------------------|---|--------------|-----|-----|------|------------|
| Gate Threshold Voltage | Q1 | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D = 250$ μ A | | 1.2 | | 2.2 | V |
| | Q2 | | | | 1.2 | | 2.2 | |
| Negative Threshold Temperature Coefficient | Q1 | $V_{GS(TH)} / T_J$ | | | | 4.5 | | mV / °C |
| | Q2 | | | | | 4.0 | | |
| Drain-to-Source On Resistance | Q1 | $R_{DS(on)}$ | $V_{GS} = 10$ V | $I_D = 10$ A | | 5.2 | 6.5 | m Ω |
| | | | $V_{GS} = 4.5$ V | $I_D = 10$ A | | 8.0 | 10 | |
| | Q2 | | $V_{GS} = 10$ V | $I_D = 20$ A | | 1.9 | 2.35 | |
| | | | $V_{GS} = 4.5$ V | $I_D = 20$ A | | 2.8 | 3.5 | |
| Forward Transconductance | Q1 | g_{FS} | $V_{DS} = 1.5$ V, $I_D = 10$ A | | | 28 | | S |
| | Q2 | | | | | 45 | | |

5. Pulse Test: pulse width ≤ 300 μ s, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

NTMFD4901NF

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

| Parameter | FET | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----|---------------------|--|-----|------|-----|------|
| CHARGES, CAPACITANCES & GATE RESISTANCE | | | | | | | |
| Input Capacitance | Q1 | C _{ISS} | V _{GS} = 0 V, f = 1 MHz, V _{DS} = 15 V | | 1150 | | pF |
| | Q2 | | | | 2950 | | |
| Output Capacitance | Q1 | C _{OSS} | | | 360 | | |
| | Q2 | | | | 1100 | | |
| Reverse Capacitance | Q1 | C _{RSS} | | | 105 | | |
| | Q2 | | | | 82 | | |
| Total Gate Charge | Q1 | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 10 A | | 9.7 | | nC |
| | Q2 | | | | 20 | | |
| Threshold Gate Charge | Q1 | Q _{G(TH)} | | | 1.1 | | |
| | Q2 | | | | 2.7 | | |
| Gate-to-Source Charge | Q1 | Q _{GS} | | | 3.3 | | |
| | Q2 | | | | 7.3 | | |
| Gate-to-Drain Charge | Q1 | Q _{GD} | | | 3.7 | | |
| | Q2 | | | 5.3 | | | |
| Total Gate Charge | Q1 | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 15 V; I _D = 10 A | | 19.1 | | nC |
| | Q2 | | | | 42.7 | | |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | | |
|---------------------|----|---------------------|---|--|-----|--|----|
| Turn-On Delay Time | Q1 | t _{d(ON)} | V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 10 A, R _G = 3.0 Ω | | 9.0 | | ns |
| | Q2 | | | | 14 | | |
| Rise Time | Q1 | t _r | | | 15 | | |
| | Q2 | | | | 16 | | |
| Turn-Off Delay Time | Q1 | t _{d(OFF)} | | | 14 | | |
| | Q2 | | | | 25 | | |
| Fall Time | Q1 | t _f | | | 4.0 | | |
| | Q2 | | | | 7.0 | | |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | | |
|---------------------|----|---------------------|--|--|-----|--|----|
| Turn-On Delay Time | Q1 | t _{d(ON)} | V _{GS} = 10 V, V _{DS} = 15 V, I _D = 10 A, R _G = 3.0 Ω | | 6.0 | | ns |
| | Q2 | | | | 10 | | |
| Rise Time | Q1 | t _r | | | 14 | | |
| | Q2 | | | | 15 | | |
| Turn-Off Delay Time | Q1 | t _{d(OFF)} | | | 17 | | |
| | Q2 | | | | 32 | | |
| Fall Time | Q1 | t _f | | | 3.0 | | |
| | Q2 | | | | 5.0 | | |

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

NTMFD4901NF

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | FET | Symbol | Test Condition | Min | Typ | Max | Unit | |
|---|-----|----------|---|---------------------------|------|------|------|--|
| DRAIN-SOURCE DIODE CHARACTERISTICS | | | | | | | | |
| Forward Voltage | Q1 | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 3\text{ A}$ | $T_J = 25^\circ\text{C}$ | 0.75 | 1.0 | V | |
| | | | | $T_J = 125^\circ\text{C}$ | 0.62 | | | |
| | Q2 | | $V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ | $T_J = 25^\circ\text{C}$ | 0.45 | 0.70 | | |
| | | | | $T_J = 125^\circ\text{C}$ | 0.37 | | | |
| Reverse Recovery Time | Q1 | t_{RR} | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 3\text{ A}$ | | 23 | | ns | |
| | Q2 | | | | 40 | | | |
| Charge Time | Q1 | | | t_a | | 12 | | |
| | Q2 | | | | | 21 | | |
| Discharge Time | Q1 | | | t_b | | 11 | | |
| | Q2 | | | | | 19 | | |
| Reverse Recovery Charge | Q1 | Q_{RR} | | 12 | | nC | | |
| | Q2 | | | 40 | | | | |

PACKAGE PARASITIC VALUES

| | | | | | | | |
|-------------------|----|-------|--------------------------|--|-------|--|----------|
| Source Inductance | Q1 | L_S | $T_A = 25^\circ\text{C}$ | | 0.38 | | nH |
| | Q2 | | | | 0.65 | | |
| Drain Inductance | Q1 | L_D | | | 0.054 | | nH |
| | Q2 | | | | 0.007 | | |
| Gate Inductance | Q1 | L_G | | | 1.5 | | nH |
| | Q2 | | | | 1.5 | | |
| Gate Resistance | Q1 | R_G | | | 0.8 | | Ω |
| | Q2 | | | | 0.8 | | |

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|-------------------|-----------------------|
| NTMFD4901NFT1G | DFN8 (Pb-Free) | 1500 / Tape & Reel |
| NTMFD4901NFT3G | DFN8 (Pb-Free) | 5000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS – Q1

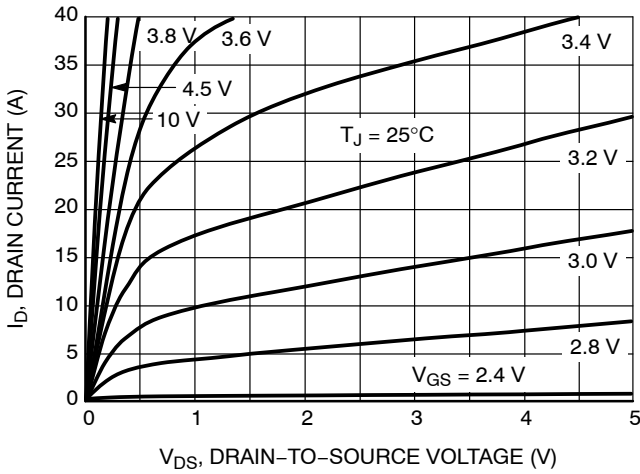


Figure 1. On-Region Characteristics

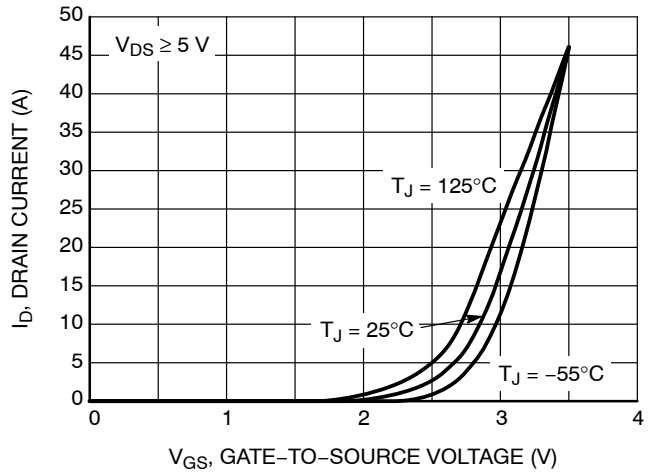


Figure 2. Transfer Characteristics

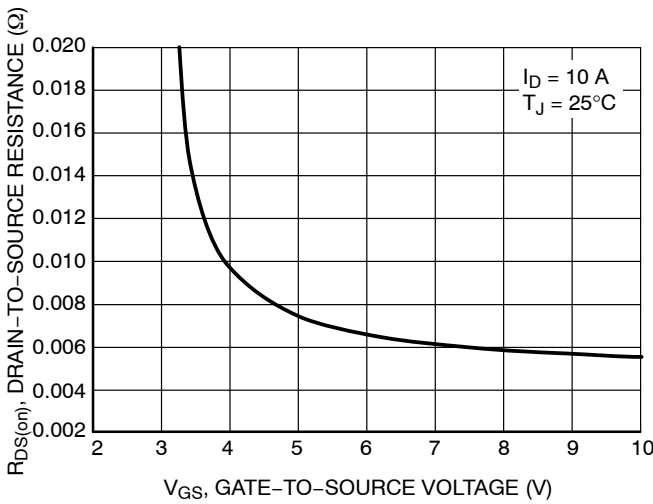


Figure 3. On-Resistance vs. Gate-to-Source Resistance

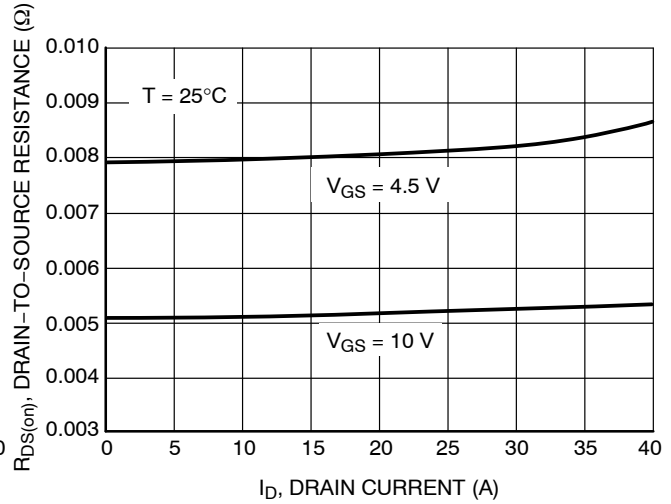


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

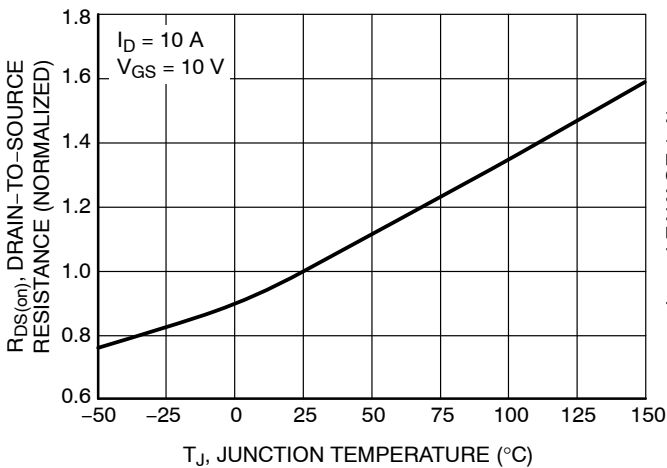


Figure 5. On-Resistance Variation with Temperature

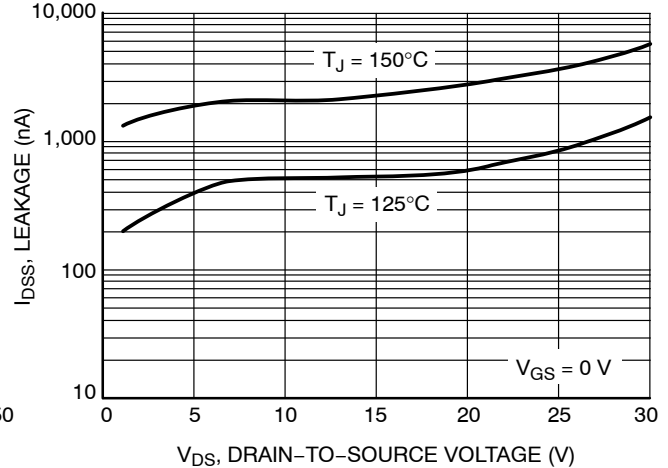


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTMFD4901NF

TYPICAL CHARACTERISTICS - Q1

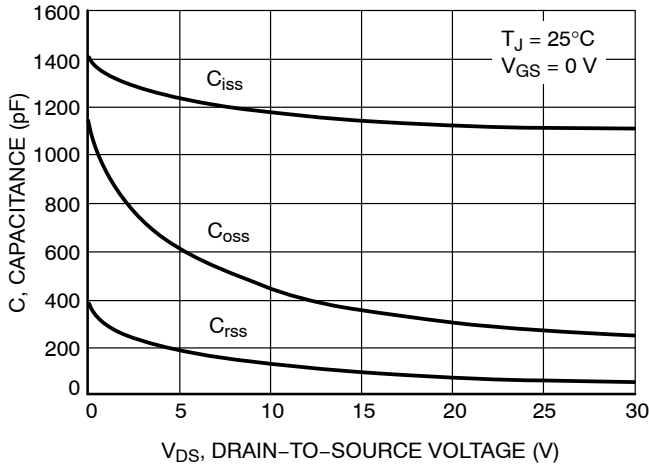


Figure 7. Capacitance Variation

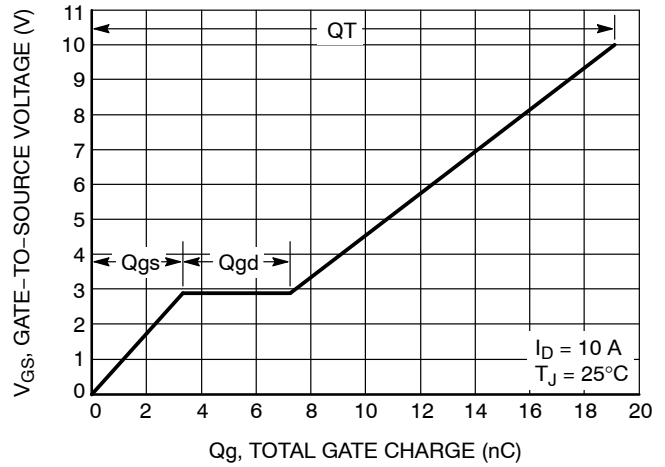


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

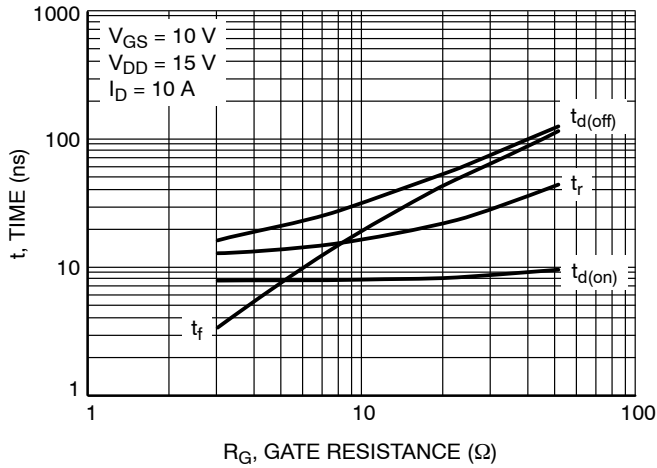


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

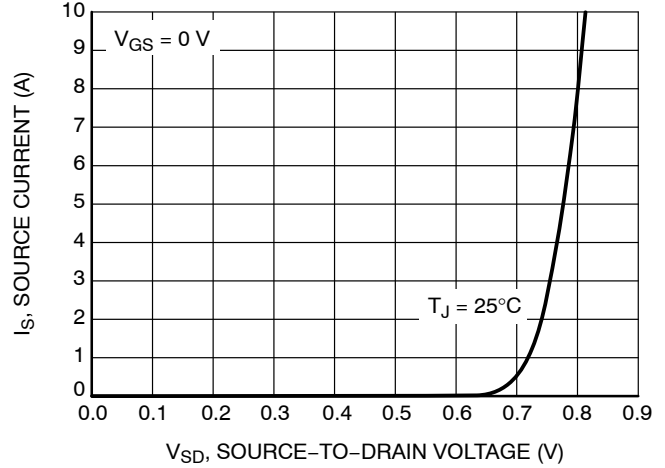


Figure 10. Diode Forward Voltage vs. Current

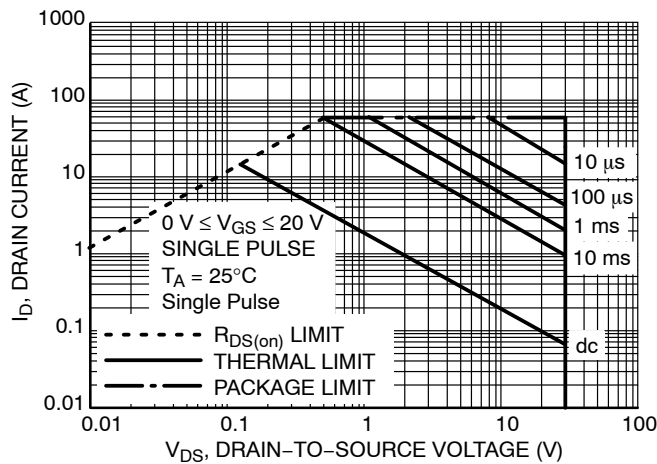


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS – Q1

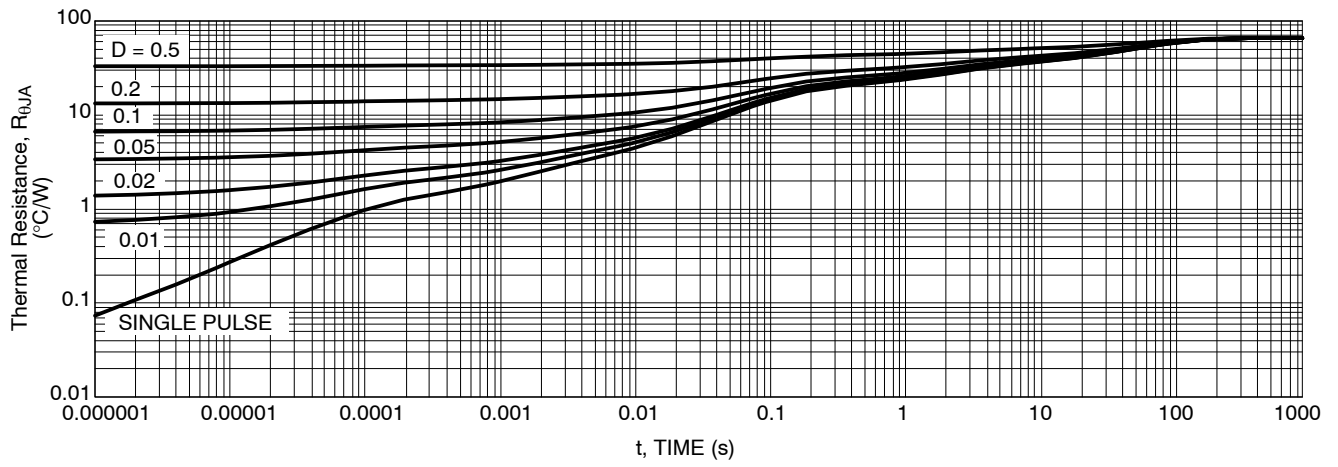


Figure 12. Thermal Response

TYPICAL CHARACTERISTICS – Q2

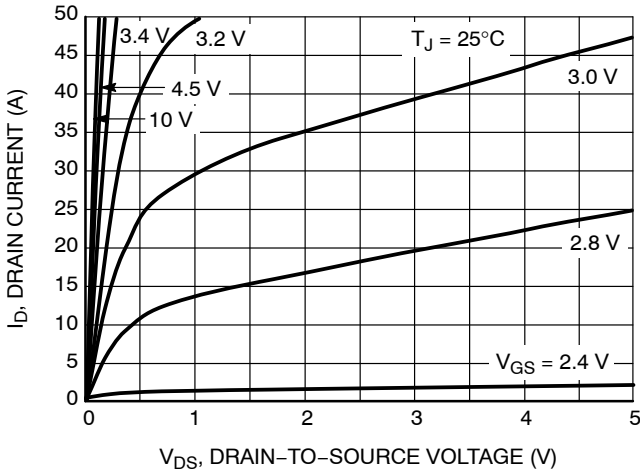


Figure 13. On-Region Characteristics

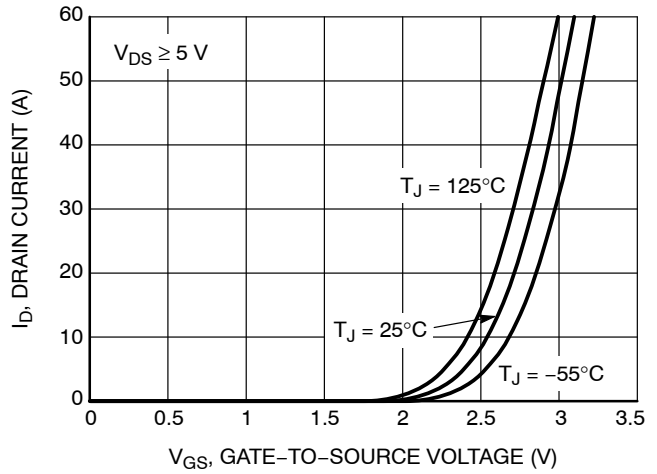


Figure 14. Transfer Characteristics

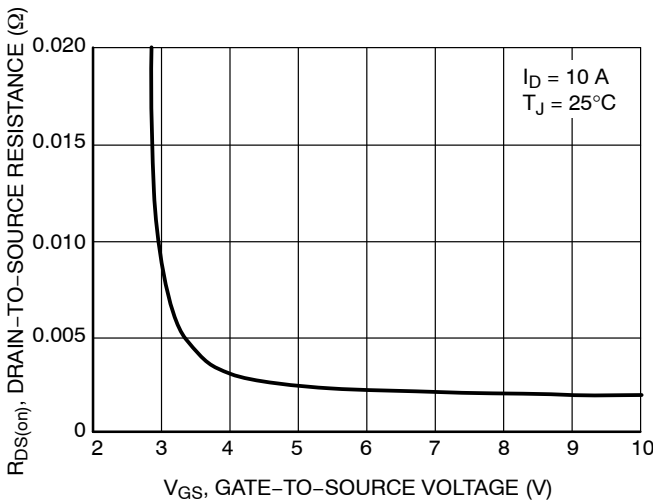


Figure 15. On-Resistance vs. Gate-to-Source Resistance

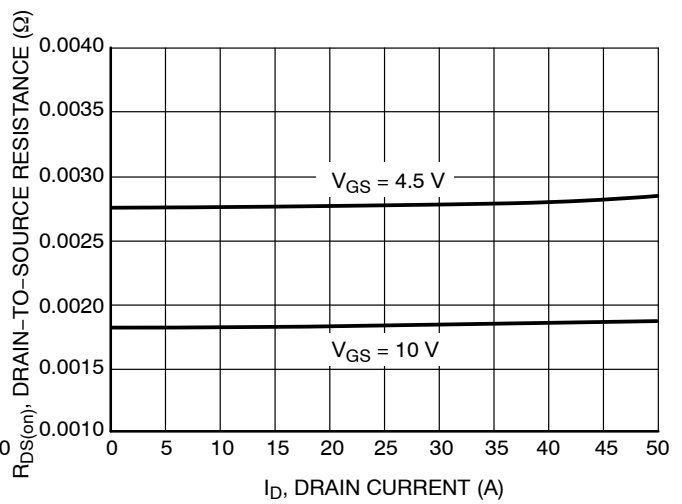


Figure 16. On-Resistance vs. Drain Current and Gate Voltage

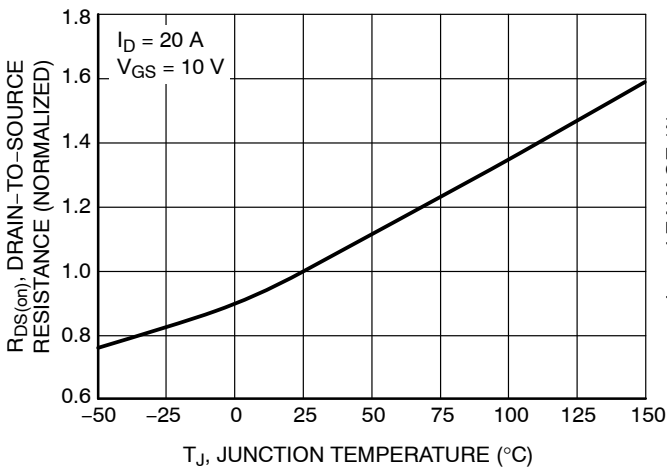


Figure 17. On-Resistance Variation with Temperature

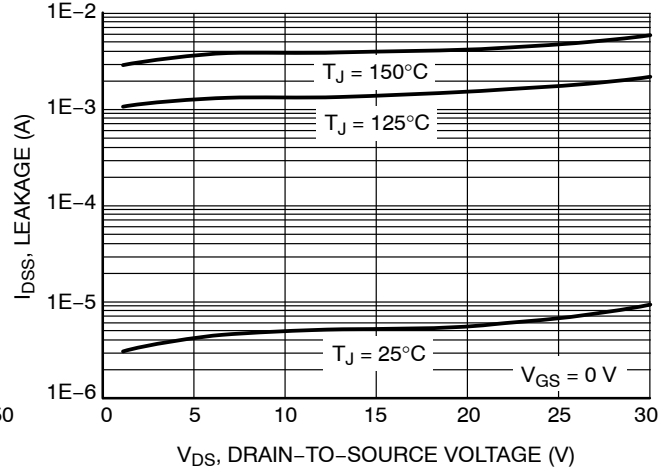


Figure 18. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS – Q2

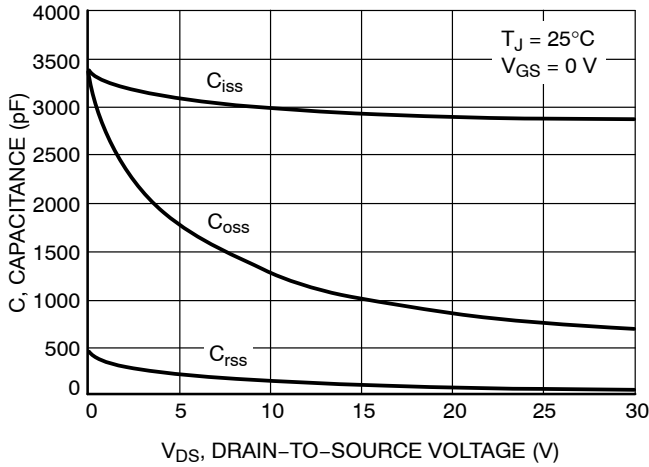


Figure 19. Capacitance Variation

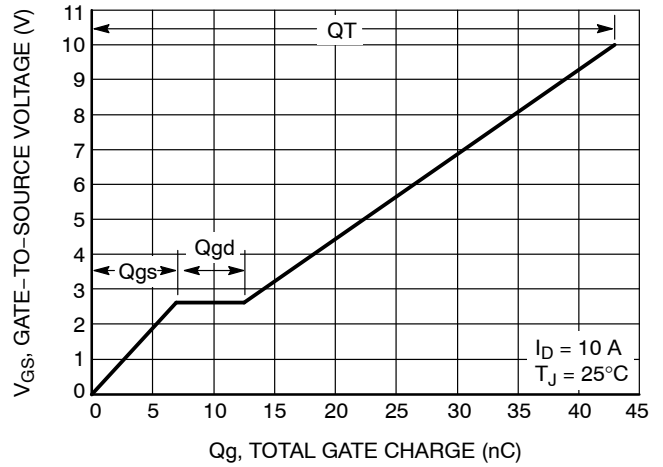


Figure 20. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

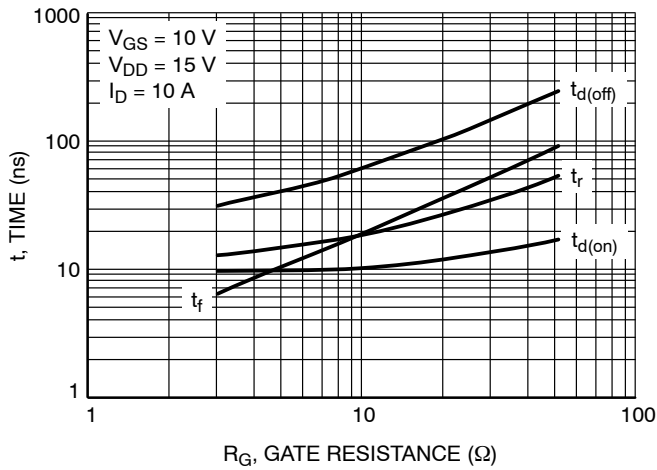


Figure 21. Resistive Switching Time Variation vs. Gate Resistance

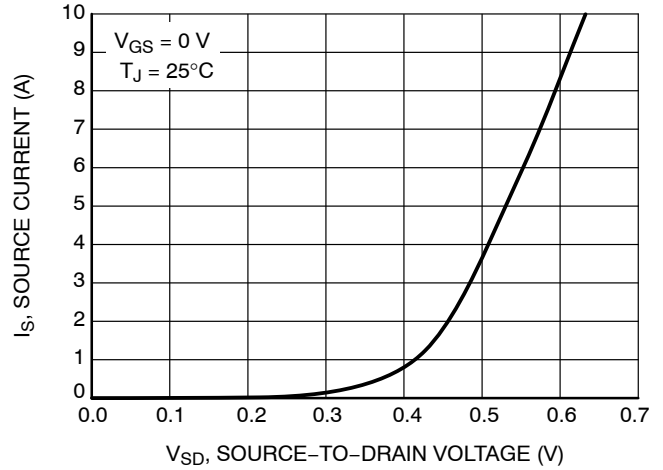


Figure 22. Diode Forward Voltage vs. Current

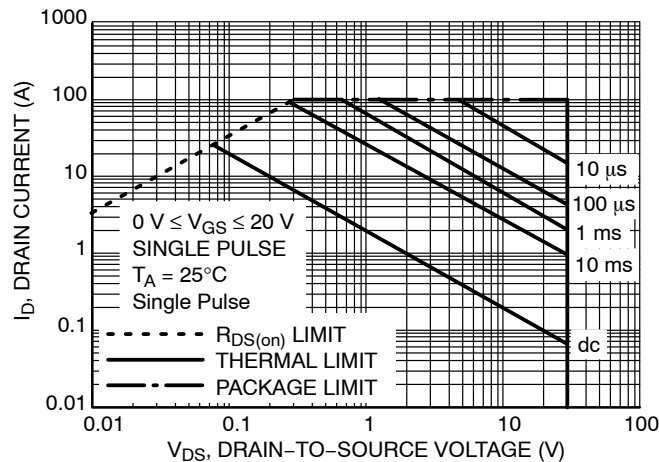


Figure 23. Maximum Rated Forward Biased Safe Operating Area

NTMFD4901NF

TYPICAL CHARACTERISTICS – Q2

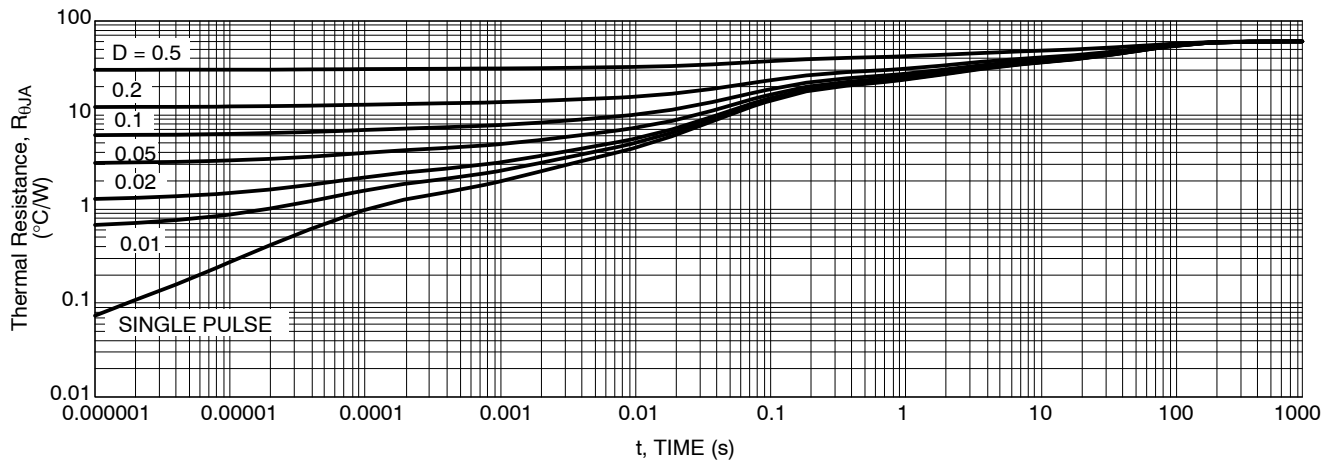
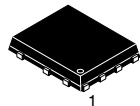


Figure 24. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

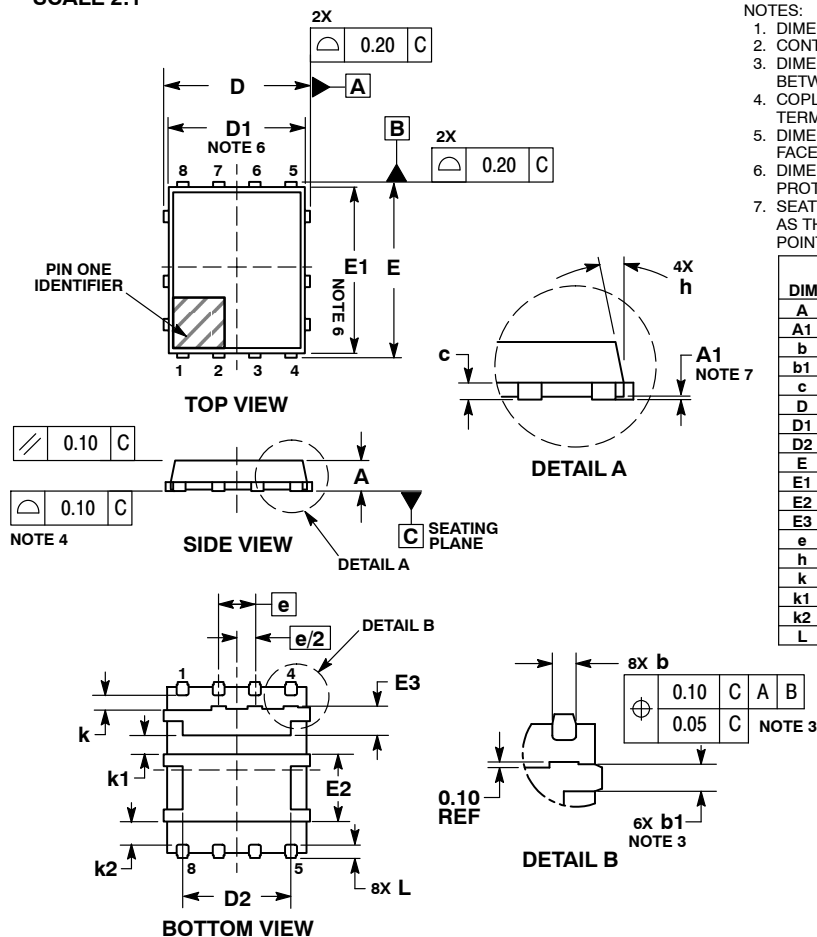


SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual-Asymmetrical)

CASE 506BX
ISSUE D

DATE 24 JUN 2014

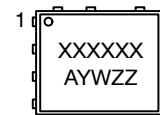


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS *b* AND *L* ARE MEASURED AT THE PACKAGE SURFACE.
6. DIMENSIONS *D1* AND *E1* DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
7. SEATING PLANE IS DEFINED BY THE TERMINALS. *A1* IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.90 | 1.10 |
| A1 | 0.00 | 0.05 |
| <i>b</i> | 0.41 | 0.61 |
| <i>b1</i> | 0.41 | 0.61 |
| <i>c</i> | 0.23 | 0.33 |
| D | 5.00 | 5.30 |
| D1 | 4.50 | 5.10 |
| D2 | 3.50 | 4.22 |
| E | 6.00 | 6.30 |
| E1 | 5.50 | 6.10 |
| E2 | 2.27 | 2.67 |
| E3 | 0.82 | 1.22 |
| <i>e</i> | 1.27 BSC | |
| <i>h</i> | --- | 12 ° |
| <i>k</i> | 0.39 | 0.59 |
| <i>k1</i> | 0.56 | 0.76 |
| <i>k2</i> | 0.73 | 0.93 |
| <i>L</i> | 0.35 | 0.55 |

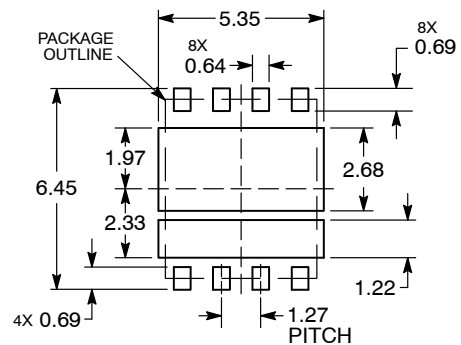
GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

- PIN 1. GATE 1
 2. DRAIN 1
 3. DRAIN 1
 4. DRAIN 1
 5. SOURCE 2
 6. SOURCE 2
 7. SOURCE 2
 8. GATE 2
 9. DRAIN 1
 10. SOURCE 1/DRAIN 2

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| DESCRIPTION: | DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL-ASYMMETRICAL) | PAGE 1 OF 1 |

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